Loongtion®

NVMe BGA SSD

Product Specification

V2.1

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Note:

The contents of this specification do not represent a commitment from the company. Due to product version upgrades or other requirements, the content of this document may be updated periodically without notice. If you require the latest version of the manual, please contact the relevant personnel of our company.

Disclaimer:

Unless otherwise agreed, this document is provided as a usage guide only. All statements, information, and recommendations in this document are made without any warranty.

Revision History

Date	Reviser	Version	Remarks
2023.01.04	Tian Yue	V1.0	Initial Specification
2023.04.02	Tian Yue	V1.1	Format Revision
2023.05.10	Tian Yue	V1.2	Version upgrade
2024.05.23	Tian Yue	V1.3	Change to new version
2024.09.29	Tian Yue	V1.4	Modify trigger pin for soft erase
2024.11.07	Tian Yue	V1.5	Add thermal performance data
2025.10.13	Wang Teng	V2.0	Added table of contents
2026.01.23	Zhao Haonan	V2.1	Modified content

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1. Introduction

1.1 Document Purpose

1) This document provides a comprehensive and detailed description of the NVMe BGA SSD parameters and electrical performance, and gives general instructions on the product's environmental adaptability and reliability.
2) This document will provide reference for engineering and technical personnel in product selection from aspects such as product capacity and product grade.

1.2 Document Scope

This document is mainly intended for engineering and technical personnel for product selection.

1.3 Terms and Abbreviations

TBW: Total Bytes Written;

POR: Power-On Reset;

MTBF: Mean Time Between Failures, average time between failures;

HMB: Host Memory Buffer, host memory cache;

1.4 Operating Conditions

Unless otherwise specified, for modules developed or produced according to this series, the recommended operating ambient temperature and storage temperature are as follows:

Table 1

Grade	Category	Operating Temperature	Storage Temperature
I	Industrial Grade	-40℃~+85℃	-45℃~+90℃
M	Military Grade	-55℃~+105℃	-55℃~+105℃

2. Product Overview

The NVMe BGA SSD uses a China-domestic NVMe controller paired with Yangtze Memory TLC NAND Flash chips. The module adopts a multi-chip stacked package design to achieve large capacity and high-speed data transfer. It is widely used in special industries such as aviation, aerospace, vehicles, and ships.

2.1 Typical Applications

- Embedded devices and systems;
- Industrial control;
- Ruggedized computer.

2.2 Product Features

- Full China-domestic design;
- Flash memory type: TLC/pSLC;

- Adopts a local-DRAM-less architecture and supports HMB function;
- Interface speed: PCIe 3.0 x4 in TLC mode, PCIe 3.0 x2 in pSLC mode, compliant with NVMe 1.4 standard protocol;
- Supports high-performance SLC capacity, direct TLC write, multiple data encryption and protection mechanisms, built-in POR function, multi-level power management, and intelligent thermal throttling.

2.3 System Configuration Requirements

- Supply voltage: DC +3.3 V / +1.2 V / +1.8 V;
- Operating systems: Windows series, Linux, Kylin V10, etc.;

2.4 Operating Principle

The main function of the NVMe BGA SSD is to fulfill user requirements for data reading and storage. The storage controller interacts with the host port via the NVMe interface for data exchange. After parsing valid data through the NVMe protocol and performing link data verification, it distributes the data to the flash memory array for storage management. The internal architecture of the NVMe interface solid-state storage drive is shown in Figure 1.

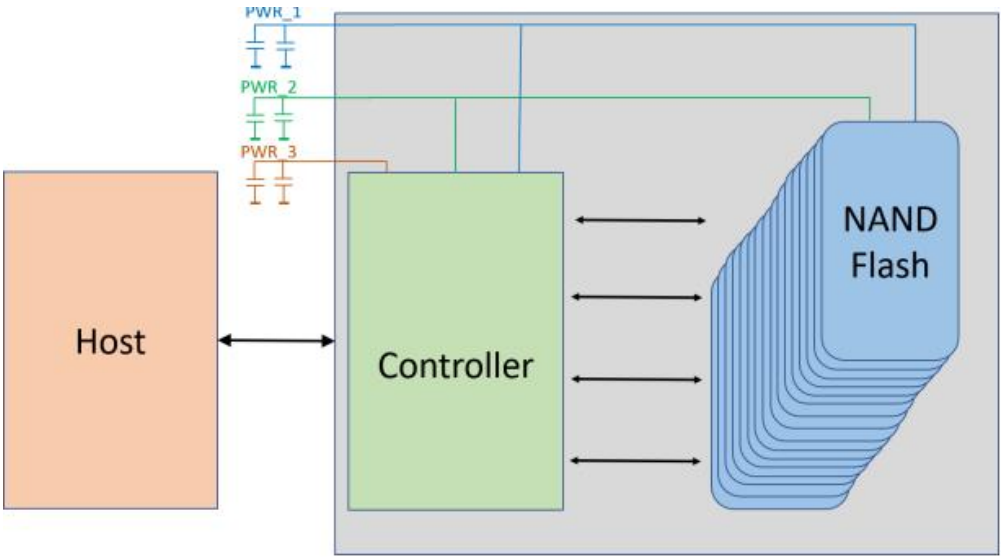


Figure 1 Internal Architecture of NVMe Interface Solid-State Storage Drive

3. Physical Characteristics

3.1 Interface Definition

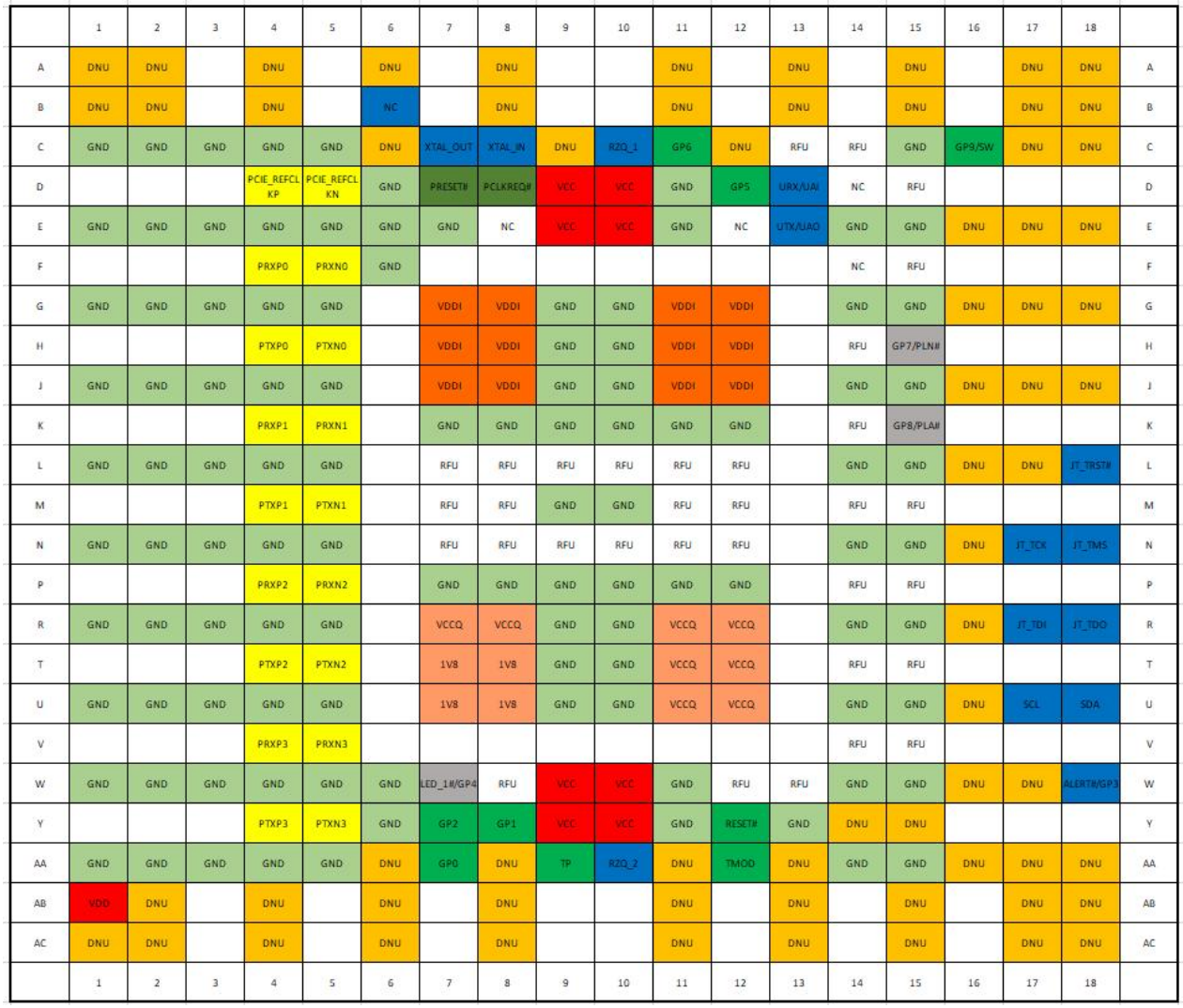


Figure 2 Pin Diagram

The electrical characteristics of this product comply with the NVMe protocol specification. The interface signal definitions are shown in Table 2.

Table 2 NVMe BGA SSD Interface Definition

Signal Name	Ball No.	Pin Type *1		Description
PCIE_REFCLKP	D4	I	PCIe Interface	PCIe Reference Clock P
PCIE_REFCLKN	D5	I		PCIe Reference Clock N
PRXP0	F4	I		PCIe Lane 0 Receive Differential Signal P
PRXN0	F5	I		PCIe Lane 0 Receive Differential Signal N
PTXP0	H4	O		PCIe Lane 0 Transmit Differential Signal P
PTXN0	H5	O		PCIe Lane 0 Transmit Differential Signal N
PRXP1	K4	I		PCIe Lane 1 Receive Differential Signal P

Note: I – Input only, O – Output only, I/O – Input and Output

Signal Name	Ball No.	Pin Type *1		Description
PRXN1	K5	I		PCIe Lane 1 Receive Differential Signal N
PTXP1	M4	O		PCIe Lane 1 Transmit Differential Signal P
PTXN1	M5	O		PCIe lane 1 transmit differential signal N
PRXP2	P4	I		PCIe lane 2 receive differential signal P
PRXN2	P5	I		PCIe lane 2 receive differential signal N
PTXP2	T4	O		PCIe lane 2 transmit differential signal P
PTXN2	T5	O		PCIe lane 2 transmit differential signal N
PRXP3	V4	I		PCIe lane 3 receive differential signal P
PRXN3	V5	I		PCIe lane 3 receive differential signal N
PTXP3	Y4	O		PCIe lane 3 transmit differential signal P
PTXN3	Y5	O		PCIe channel 3 transmitter differential signal N
CLKREQ#	D8	I/O		PCIe clock request, active low
PERST#	D7	I		PCIe hardware reset, active low
XTAL_OUT	C7	O	Crystal oscillator	Crystal oscillator output
XTAL_IN	C8	I		Crystal oscillator input
RZQ_1	C10	N/A	ZQ	NAND calibration resistor
RZQ_2	AA10	N/A		Memory or NAND calibration resistor
RESET#	Y12	I	Reset	Power-on reset, active low.
TMOD	AA12	I	Test	ATE test mode selection
TP	AA9	O		Analog test output
GP0	AA7	I/O	Debug GPIO (1.8V)	General purpose input/output 0
GP1	Y8	I/O		General purpose input/output 1
GP2	Y7	I/O		General-purpose input and output 2, secure erase
ALERT#/GP3	W18	I/O		Sends alert notification to host (output, active low) / General-purpose input and output 3
LED_1#/GP4	W7	I/O		Output signal to drive external transistor through LED device for status indication (output, active low) / General-purpose input and output 4
GP5	D12	I/O		General-purpose input and output 5
GP6	C11	I/O		General-purpose input/output 6
GP7/PLN#	H15	I/O		General-purpose input and output 7 / Power-down notification (input, active low)
GP8/PLA#	K15	I/O		GPIO8 / Power-down Acknowledge (output, active low)
GP9	C16	I/O		GPIO9

Signal Name	Ball No.	Pin Type *1		Description
SDA	U18	I/O	I^2C/ SMBus (1.8V)	I2C Data / SMBus Data, open-drain
SCL	U17	I/O		I2C Clock / SMBus Clock, open-drain
UTX/UAO	E13	O	UART (1.8V)	UART Transmit / UART Output
URX/UAI	D13	I		UART Receive / UART Input
JT_TMS	N18	I	JTAG (1.8V)	JTAG Mode Select
JT_TDI	R17	I		JTAG Data Input
TRST#	L18	I		JTAG reset, active low
JT_TDO	R18	O		JTAG data output
JT_TCK	N17	I		JTAG clock
VCC	D9, D10, E9, E10, W9, W10, Y9, Y10	Power (3.3 V)		External power supply
VCCQ	R7, R8, R11, R12, T11, T12, U11, U12	Power (1.2 V / 1.8 V)		External power supply
VDDI	G7, G8, G11, G12, H7, H8, H11, H12, J7, J8, J11, J12	Power (1.2V)		LDO supply
VDD	AB1	Power (0.9V)		LDO output – core supply
1V8	T7, T8, U7, U8	Power (1.8V)		Power supply for PCIe, PLL, digital inputs and outputs, for ATE use
GND	C1, C2, C3, C4, C5, C15, D6, D11, E1, E2, E3, E4, E5, E6, E7, E11, E14, E15, F6, G1, G2, G3, G4, G5, G9, G10, G14, G15, H9, H10, J1, J2, J3, J4, J5, J9, J10, J14, J15, K7, K8, K9, K10, K11, K12, L1, L2, L3, L4, L5, L14, L15, M9, M10, N1, N2, N3, N4, N5, N14, N15, P7, P8, P9, P10, P11, P12, R1, R2, R3, R4, R5, R9, R10, R14, R15, T9, T10, U1, U2, U3, U4, U5, U9, U10, U14, U15, W1, W2, W3, W4, W5, W6, W11, W14, W15, Y6, Y11, Y13, AA1, AA2, AA3, AA4, AA5, AA14, AA15	Ground		Ground

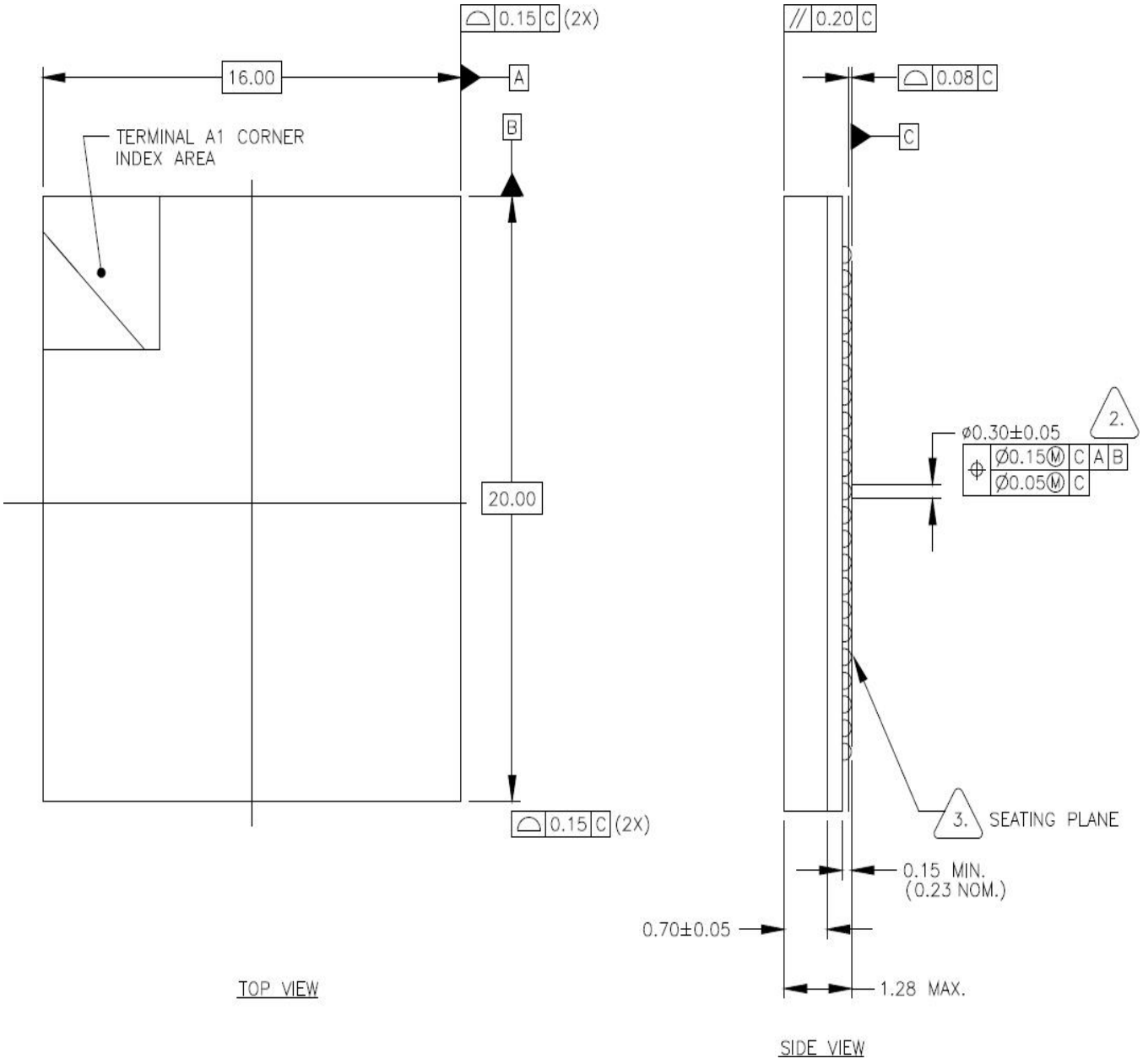
Signal Name	Ball No.	Pin Type *1	Description
DNU	A1, A2, A4, A6, A8, A11, A13, A15, A17, A18, B1, B2, B4, B8, B11, B13, B15, B17, B18, C6, C9, C12, C17, C18, E16, E17, E18, G16, G17, G18, J16, J17, J18, L16, L17, N16, R16, U16, W16, W17, Y14, Y15, AA6, AA8, AA11, AA13, AA16, AA17, AA18, AB2, AB4, AB6, AB8, AB11, AB13, AB15, AB17, AB18, AC1, AC2, AC4, AC6, AC8, AC11, AC13, AC15, AC17, AC18	NC	No Connect
NC	B6, D14, E8, E12, F14	NC	No Connect
RFU	C13, C14, D15, F15, H14, K14, L7, L8, L9, L10, L11, L12, M7, M8, M11, M12, M14, M15, N7, N8, N9, N10, N11, N12, P14, P15, T14, T15, V14, V15, W8, W12, W13	NC	Reserved
Note: For differential signal pairs (e.g., RX0P and RX0N), 'P' and 'N' denote positive and negative signals respectively. For signals containing '#' in their names, such as CLKREQ#, PERST#, RESET#, and JT_TRST#, '#' indicates active-low.			

3.2 Weight

Total weight <10 g.

3.3 Mechanical Dimensions

The mechanical dimensions are: 20 mm (L) × 16 mm (W) × 1.28 mm (H). The physical dimensions are shown in Figure 3 (units in mm):


0.15 C (2X)
16.00
A
B
TERMINAL A1 CORNER
INDEX AREA
20.00
0.15 C (2X)
TOP VIEW
// 0.20 C
0.08 C
C
ø0.30±0.05
2.
Ø0.15Ⓜ C A B
Ø0.05Ⓜ C
3.
SEATING PLANE
0.15 MIN.
(0.23 NOM.)
0.70±0.05
1.28 MAX.
SIDE VIEW

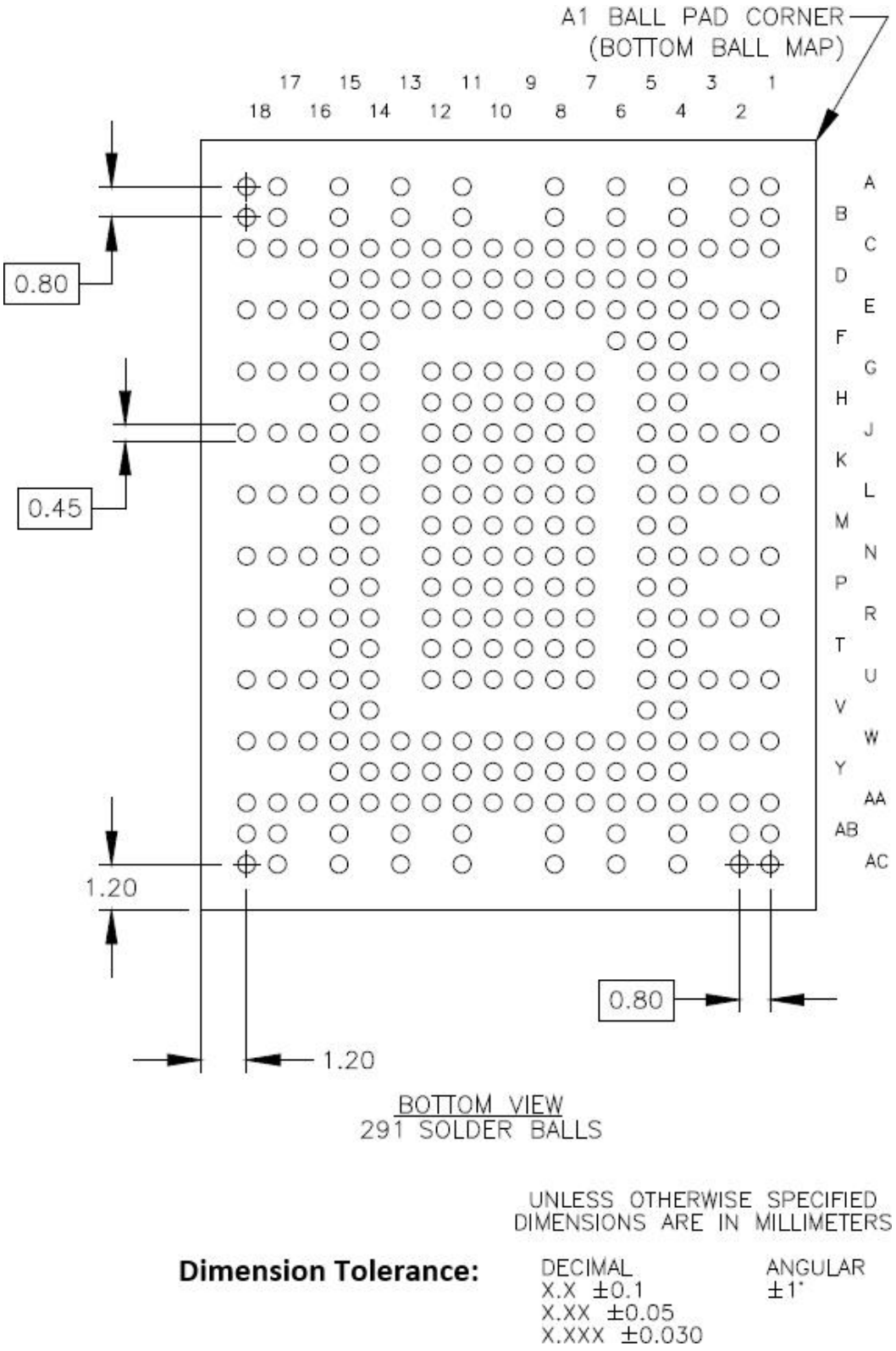


Figure 3 NVMe BGA SSD Dimensions

Length (mm)	Width (mm)	Height (mm)
20±0.1	16±0.1	1.3±0.1

4. Performance Parameters

4.1 Supply Voltage

Table 3 Supply Voltage Parameters

Operating Supply	Voltage Value			Unit
	Min	Typ	Max	V
VCC	2.97	3.3	3.63	V
VCCQ	1.14	1.2	1.26	V
VDDI	1.14	1.2	1.26	V
1V8	1.71	1.8	1.89	V

4.2 Product Capacity

Table 4 Product Capacity

Nominal Capacity	Actual Capacity
32 GB	29 GB
64 GB	59 GB
128 GB	119 GB
256 GB	238 GB
512 GB	476 GB

The tolerance between nominal capacity and actual capacity is ±10%.

4.3 Thermal Performance Data

Table 5 Thermal Performance Data

Parameter	Value	Unit	Description
θJA[1]	26.84	℃/W	$\theta_{JA}=(T_J-T_A)/P_H$
ψJT[2]	0.25	℃/W	ψJT=(TJ-TT)/PD
θ_{JC}*53	9.71	℃/W	θJC=(TJ-TC)/PD
ψ_{JB}*54	11.33	℃/W	ψJB=(TJ-TB)/PD

θJA is the junction-to-ambient thermal resistance (EIA/JESD51-2 and EIA/JESD51-6), representing the resistance to heat flow from the chip to the surrounding air. It is a parameter used to indicate the package's heat dissipation capability. A smaller θJA means better overall thermal performance.

ψJT is the junction-to-top center thermal characterization parameter (EIA/JESD51-2, EIA/JESD51-6), used to estimate junction temperature by measuring top temperature in the actual environment.

θJC is the junction-to-case thermal resistance, representing the resistance to heat flow from the die to the package top case. θJC can be used in a dual-resistor thermal model. θJC is an important parameter when an external heat sink is attached to the package top.

ψJB is the junction-to-board thermal characterization parameter. If the package has no external heat sink attached, ψJB is an important parameter indicating the temperature difference between the junction and the board. θJB can be used in a dual-resistor model.

4.4 Transfer Speed

Table 5 Technical Specifications (TLC)

	Capacity	256GB(TLC)	512GB(TLC)
Performance	4KB Random Read (IOPS)	15K	15K
	4KB Random Write (IOPS)	120K	120K
	128KB Sequential Read (MB/s)	1100	1100
	128KB Sequential Write (MB/s)	550	550
Test Platform: Intel Core i3, GIGABYTE GA-B250-D3A, 8GB DDR3; Test Environment: Room Temperature 25°C. Test System: Windows 10 Professional Test software: ATTO (file size 4GB), queue depth: 4.			

***Test speed is for reference only.**

Table 6 Technical Parameters (pSLC)

	Capacity	32GB(pSLC)	64GB(pSLC)	128GB(pSLC)
Performance	4KB Random Read (IOPS)	20K	20K	20K
	4KB Random Write (IOPS)	120K	120K	120K
	128KB Sequential Read (MB/s)	1200	1200	1200
	128KB Sequential Write (MB/s)	1300	1300	1300
Test Platform: CPU i3, GIGABYTE GA-B250-D3A, 8 GB DDR3; Test Environment: Room temperature 25°C. Test System: Windows 10 Professional Test software: ATTO (file size 4GB), queue depth: 4.				

***Test speed is for reference only.**

4.5 Power Consumption

Table 7 Power Consumption Parameters

Power Consumption	512GB(TLC)	256GB(TLC)	128GB(pSLC)	64GB(pSLC)	32GB(pSLC)
Sequential Write Power	≤3.1W	≤3.0W	≤3.1W	≤2.5W	≤2.1W
Sequential Read Power	≤2.7W	≤2.6W	≤2.7W	≤2.1W	≤1.6W

4.6 Ordering Information

Table 8 Ordering Information and Configuration

Grade	Nominal Capacity	Product Model		Mode/Protocol
		TLC	pSLC	
Industrial Grade (-40/85)	32GB	/	YIDF032NMS-S	PCIe3.0*2 /NVMe 1.4 Protocol
	64GB	/	YIDF064NMS-S	
	128GB	/	YIDF128NMS-S	
	256GB	YIDF256NMS-S	/	PCIe3.0*4 /NVMe 1.4 Protocol
	512GB	YIDF512NMS-S	/	
Wide Temperature Grade (-55/105)	64GB	/	YMDF64NMS-S(Screened)	PCIe3.0*2 /NVMe 1.4 Protocol
	128GB	/	YMDF128NMS-S(Screened)	

4.7 Endurance (TBW)

Table 9 Product Endurance

Nominal Capacity	Data Written (TLC Mode)	Data Write Volume (pSLC Mode)
32GB	/	150TB
64GB	/	300TB
128GB	/	600TB
256GB	200TB	/
512GB	400TB	/

*Data Write Volume tolerance ±10%

5. Delivery Preparation

5.1 Packaging Requirements

The product is packaged in anti-static bags. The packaging shall be clean, dry, and provide effective protection for the product.

The product packaging box shall contain anti-static foam, a certificate of quality, and the corresponding test report.

5.2 Transportation

a) The packed products may be transported using ordinary means of transport. During transportation, appropriate protection against rain and snow shall be provided.

b) Do not transport together with corrosive substances such as acids and alkalis.

c) Do not stack heavy objects on top of the product.

d) Handle with care during movement.

5.3 Storage

The product should be stored in a dedicated warehouse with a temperature of 0°C to 35°C, relative humidity no greater than 80%, and no strong magnetic fields. The product must not be stored together with acids, alkalis, or corrosive materials.