

Loongtion®

LPDDR4X SDRAM
Data Sheet

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Revision History

Revision	Date	Description
Rev 1.0	2024/7/16	Preliminary
Rev 1.1	2024/12/29	Content layout modification
Rev 2.0	2025/04/25	Added 8GB LPDDR4X product, modified internal block diagram
Rev 2.1	2025/11/14	Modified low-voltage DC operating conditions
Rev 3.0	2025/12/11	Added industrial/military-grade 2GB and 4GB LPDDR4X product models
Rev 3.1	2025/12/31	Modified package information
Rev 3.2	2026/03/02	Added 16-bit width

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1. Introduction

This chip is encapsulated using wafers from ChangXin Memory Technologies. It is based on traditional DDR SDRAM technology but offers significant improvements in power consumption and performance. First, power consumption is reduced through lower operating voltage, dynamic power management, Deep Sleep Mode, etc. Second, the chip provides a high data transfer rate, achieving higher bandwidth than traditional DDR through a multi-channel architecture and high clock frequency. Third, the entire package design meets China-domestic supply requirements and can provide corresponding China-domestic certification documents.

2. Product List

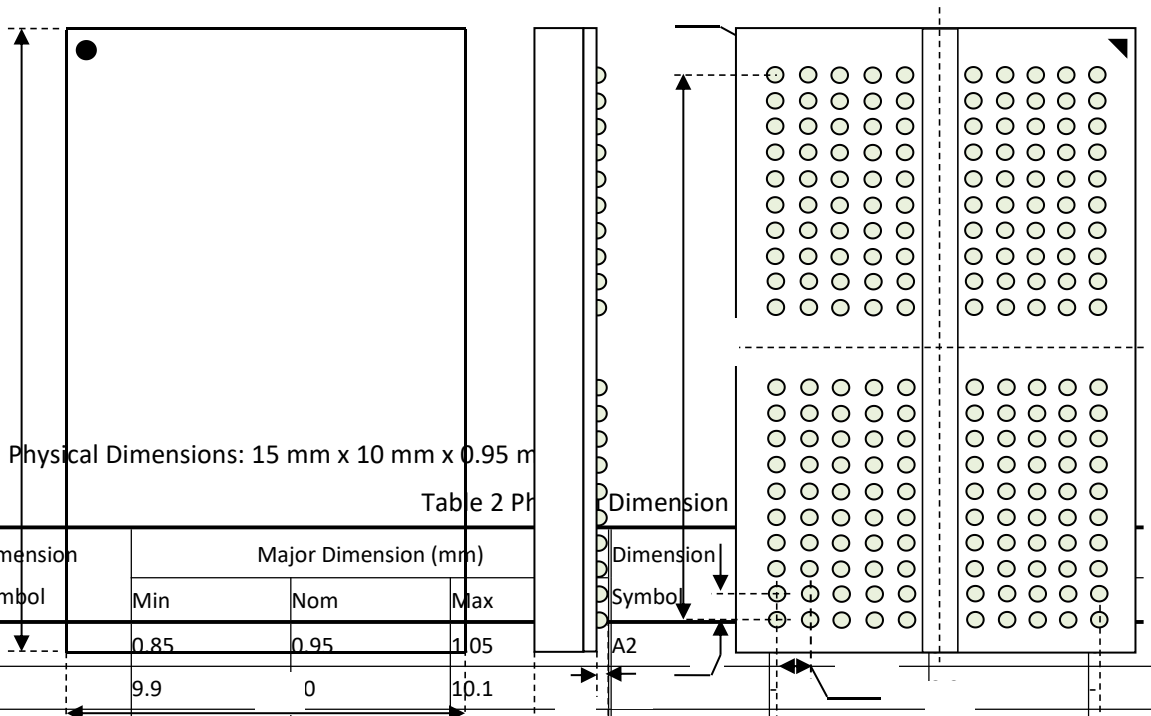
Table 1 Product Package Information

Capacity	Part Number	Package	Data Rate	Temperature Range
2GB	YMDB5CCBM-EA-A	FBGA200	3733/4266 MT/s	-55-105℃
4GB	YMDB6CCBM-EA-A	FBGA200	3733/4266Mbps	-55-105℃
2GB	YZDB5CCBM-EA-A	FBGA200	3733/4266Mbps	-40-85℃
4GB	YZDB6CCBM-EA-A	FBGA200	3733/4266Mbps	-40-85℃
	YZDB6CBAM-MA-B		3733/4266Mbps	
8GB	YZDB6CCDM-EA-A	FBGA200	3733/4266Mbps	-40-85℃

3. Product Features

3.1 Physical Characteristics

-



- Physical Dimensions: 15 mm x 10 mm x 0.95 m

Table 2 Ph Dimension

Dimension Symbol	Major Dimension (mm)			Dimension Symbol			
	Min	Nom	Max				
A1	0.85	0.95	1.05	A2			
D	9.9	0	10.1				
E	14.90	15	15.10	E1		13.65	
d	-	0.80	-	e	-	0.65	-
b	0.26	0.31	0.36				

3.2 Pin Assignments and Definitions

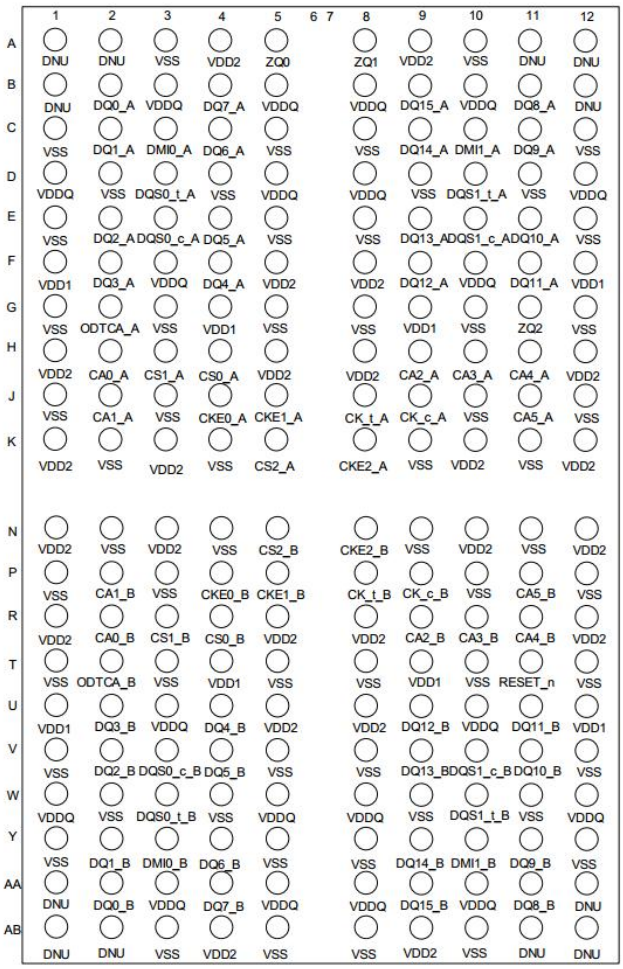


Figure 2 Pin Configuration Diagram

Note:

- **0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows, using 0.80mm pitch.**
- Top view, A1 at top-left corner. For 2GB die, CS1_A/B, CE1_A/B, and ZQ1 are no connects.
- Chip-defined VSS and VSSQ signals can be merged into a single VSS signal.
- Package requires dual-channel die or functionally equivalent single-channel die stacking.

Table 3 Pin Description Table

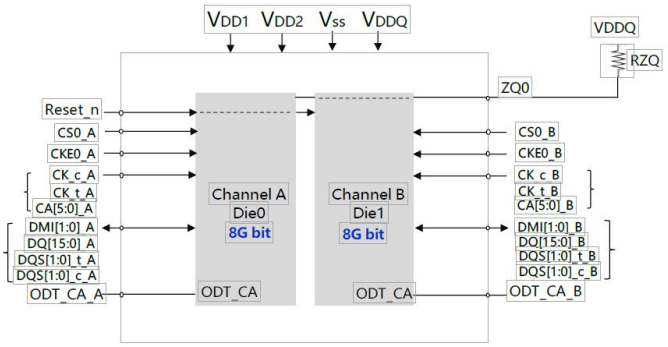
Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled at the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timing of CA parameters is referenced to CK. Each channel (A and B) has its own clock pair.
CKE_A CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A and B) has its own CKE signal.
CS_A CS_B	Input	Chip Select: CS is part of the command code. Each channel (A and B) has its own CS signal.

CA[5:0]_A, CA[5:0]_B CA[5:0]_A, CA[5:0]_B	Input	Command/Address Input: CA signals provide command and address inputs according to the command truth table. Each channel (A and B) has its own CA signals.
DQ[15:0]_A, DQ[15:0]_B DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe DQS_t and DQS_c are bidirectional differential clock signals used to strobe data during read or write operations. The data strobe is generated by the DRAM during reads and is edge-aligned with the data. The data strobe is generated by the memory controller during writes and must precede the data. Each data byte has one pair of data strobe signals. Each channel (A and B) has its own DQS signals.
DMI[1:0]_A DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bidirectional signal that is driven high when data on the data bus is inverted, and driven low when data is in normal state. Data inversion can be disabled via the Mode Register. Each data byte has one DMI signal. Each channel (A and B) has its own DMI signal. This signal is also used together with DQ signals to provide write data masking information to the DRAM. The function of the DMI pin (data inversion or data masking) depends on the Mode Register settings.
ZQ	Reference	Calibration reference: Used to calibrate output drive strength and termination resistance. Each device has one ZQ pin. The ZQ pin should be connected to VDDQ through a 240Ω ± 1% resistor.
VDDQ, VDD1, VDD2	Power	Power: Isolated on-chip to improve noise immunity.
VSS, VSSQ	Ground	Ground reference: Power ground reference
RESET_n	Input	Reset: When RESET_n is LOW, the entire chip is reset. Each chip has one RESET_n pad.
ODT_CA_A,ODT_CA_B	Input	CA ODT Control: For LPDDR4, the ODT_CA pin is used together with the mode register to turn on/off on-die termination for CA pins. For LPDDR4X, LPDDR4X devices ignore the ODT_CA pin. The ODT_CS/CA/CK functions are fully controlled by MR11 and MR22. The ODT_CA pin should be connected to VDD2 or VSS.

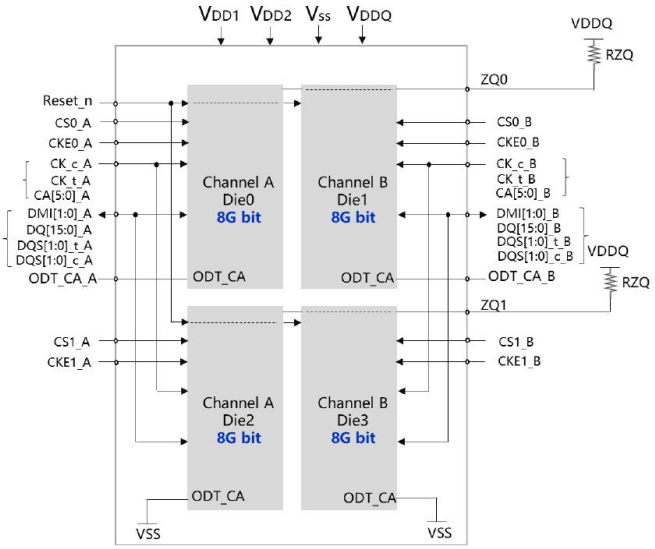
Note:

"_A" and "_B" denote DRAM channels. The "_A" pads are present on all devices, while "_B" pads exist only on dual-channel SDRAM devices.

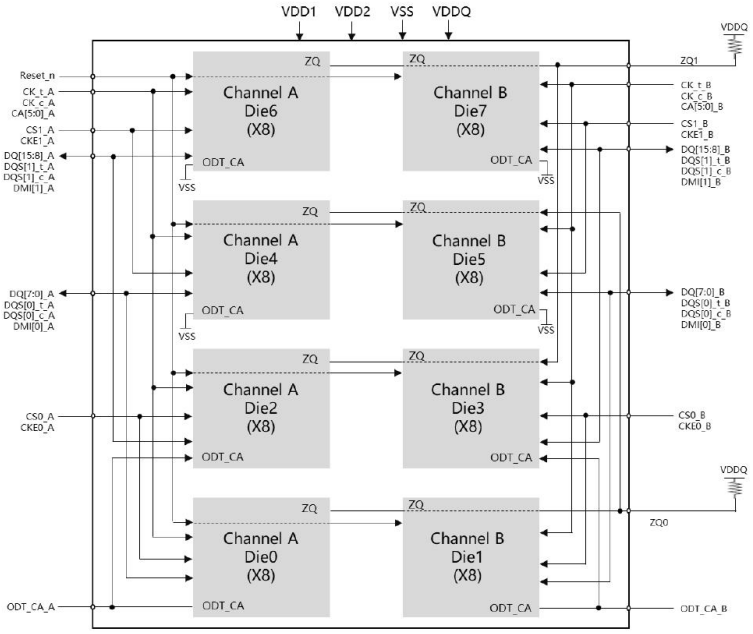
4. Internal Block Diagram



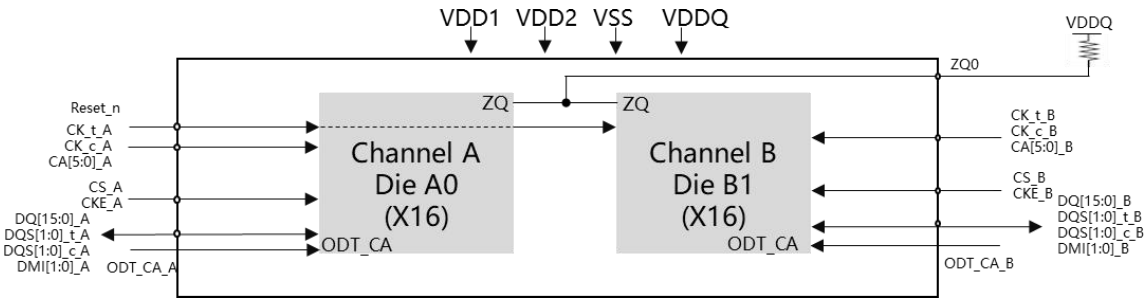
2GB 双die 双通道 单RANK



4GB 4die 双通道，双RANK



8GB 8die 双通道 双RANK



4GB Dual-Die Dual-Channel Single Rank

Figure 3 Internal Connection Diagram

5. Absolute Maximum DC Ratings

This section specifies the absolute maximum DC ratings. Stresses beyond those listed may cause permanent damage to the device.

These are stress ratings only. Operation at maximum rating conditions for extended periods may affect device reliability.

Table 4 Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit
VDD1 Supply Voltage	V_{DD1}	-0.4	2.1	V
VDD2 Supply Voltage	V_{DD2}	-0.4	1.5	
VDDQ supply voltage	V_{DDQ}			
Other pins	V_{IN} ,V_{OUT}			
Storage temperature	T_{STG}	-55	125	℃

6. AC and DC Operating Conditions

This chapter specifies four key conditions for reliable, safe, and legal operation of the low-power device: DC operating voltages, input/output leakage currents, temperature, and single-ended and differential output slew rates.

6.1 Recommended Low-Voltage DC Operating Conditions

Table 5 Recommended DC Operating Conditions

Voltage Name	Symbol	Min	Typ	Max	Unit
Core Voltage 1	V_{DD1}	1.7	1.8	1.95	V
Core Voltage 2	V_{DD2}	1.06	1.1	1.17	V
I/O Supply Voltage	V_{DDQ}	0.57	0.6	0.65	V

6.2 Input Leakage Current

Table 6 Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit
Input Leakage Current	I_L	-4	4	uA

6.3 Input/Output Leakage Current

Table 7 Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit
Input/Output Leakage Current	I_{OZ}	-5	5	uA

6.4 Operating Temperature Range

Table 8 Operating Temperature Range

Parameter/Condition	Parameter/Condition	Min	Max	Unit
Standard	T_{OPER}	-40	85	℃
Extended		85	105	℃
Note:				
1. Operating temperature is defined as the case surface temperature at the center top of the LPDDR4X device. For measurement conditions, refer to JESD51-2.				
2. Some applications require the LPDDR4X to operate at the maximum temperature condition in the high-temperature range between 85°C and 105°C case temperature. The LPDDR4X chip itself requires derating to operate in this temperature range. See MR4 (Mode Register 4) for details.				
3. Either the chip case temperature rating or the temperature sensor can be used to set the appropriate refresh rate, determine if AC timing derating is required, and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may exceed the TOPER rating applicable to the standard or high-temperature range. For example, when the temperature sensor indicates a temperature below 85°C, TCASE may be above 85°C.				

6.5 Single-Ended Output Slew Rate

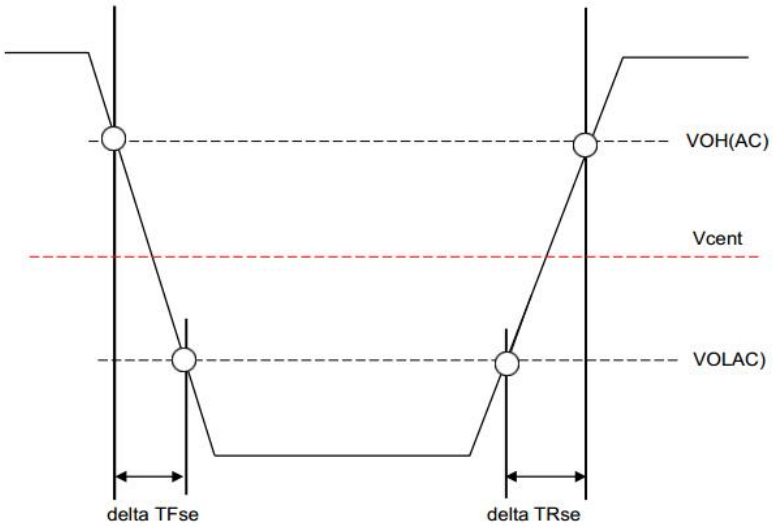


Figure 4 Single-Ended Output Slew Rate

Table 9 LPDDR4X Single-Ended Output Slew Rate (0.6 VDDQ)

Parameter	Symbol	Reference Value		Unit
		Max	Min	
Single-Ended Output Slew Rate (VOH=VDDQ*0.5)	SRQse	3	9	V/ns
Output Slew Rate Matching Ratio (Rising Edge to Falling Edge)	-	0.8	1.2	-
SR: Slew Rate, Q: Data Output (similar to DQ pin data output function), se: Single-ended Signal				
Note:				
1. Measured using output reference load.				
2. Over the full temperature and voltage range, the ratio of pull-up to pull-down slew rate is specified at the same temperature and voltage. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.				
3. Output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2*VOH(DC) and VOH(AC) = 0.8*VOH(DC).				

6.6 Differential Output Slew Rate

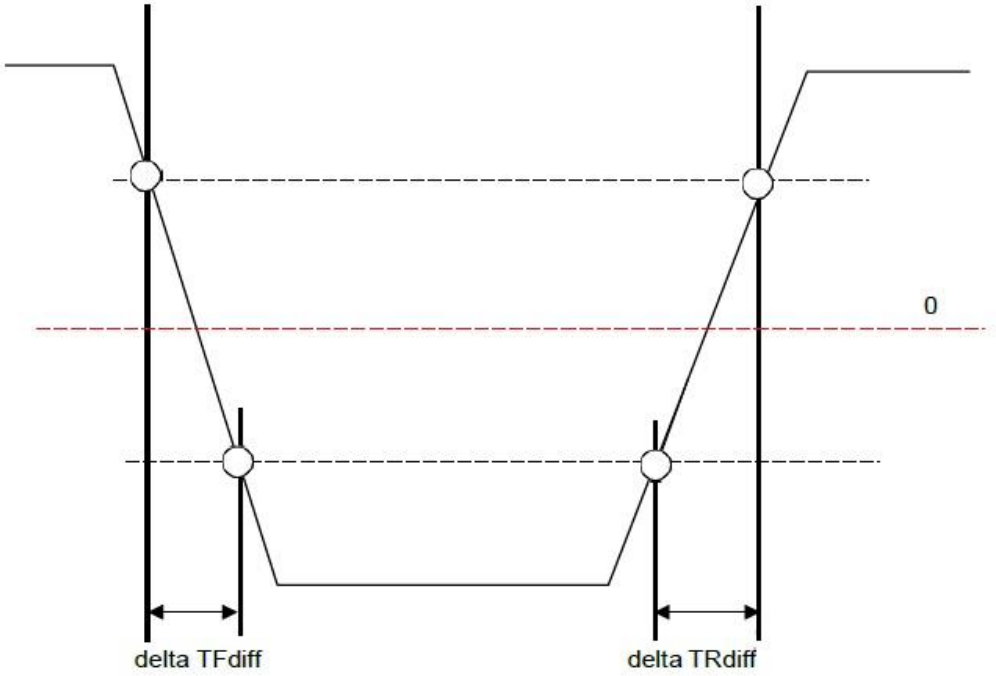


Figure 5 Differential Output Slew Rate

Table 10 Differential Output Slew Rate Table

Parameter	Symbol	Reference Value		Unit
		Max	Min	
Differential Output Slew Rate (VOH = VDDQ/3)	SRQdiff	7	18	V/ns
SR: Slew Rate, Q: Query Output (similar to data input/output in DQ), se: single-ended signal				
Note:				
1. Measured with output reference load.				

2. The ratio of pull-up to pull-down slew rate is specified as the ratio at the same temperature and voltage across the full temperature and voltage range. For a given output, it represents the maximum difference between the pull-up and pull-down drivers due to process variation.
3. Output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2 * VOH(DC) and VOH(AC) = 0.8 * VOH(DC).

7. AC and DC Input/Output Measurement Levels

This section defines the DC electrical characteristics, AC overshoot and undershoot specifications, differential input voltage specifications, and output drivers for input signals to ensure proper operation of the LPDDR4X SDRAM.

7.1 1.1V High-Speed LVCMOS (HS_LVCMOS)

7.1.1 DC Electrical Characteristics

1) CKE Input Level

Table 11 CKE Input Level

Parameter	Symbol	Min	Max	Unit
Input High Level (AC)	V_{IH}(AC)	0.75*V_{DD2}	V_{DD2}+0.2	V
Input Low Level (AC)	V_{IL}(AC)	-0.2	0.25*V_{DD2}	V
Input High Level (DC)	V_{IH}(DC)	0.65*V_{DD2}	V_{DD2}+0.2	V
Input Low Level (DC)	V_{IL}(DC)	-0.2	0.2*VDD2	V
Note:				
Refer to AC overshoot and undershoot for VIH(AC) and VIL(AC);				

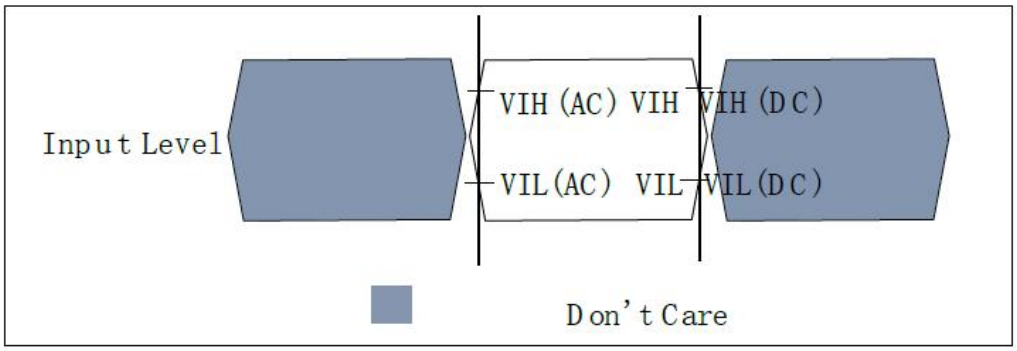


Figure 6 CKE AC Timing Definition

2) Reset_n and ODT_CA Input Levels

Table 12 Reset_n and ODT_CA Input Levels

Parameter	Symbol	Min	Max	Unit
Input High Level (DC)	V_{IH}	0.80*V_{DD2}	V_{DD2}+0.2	V
Input Low Level (DC)	V_{IL}	-0.2	0.2*V_{DD2}	V
Note: Refer to AC overshoot and undershoot for VIH and VIL;				

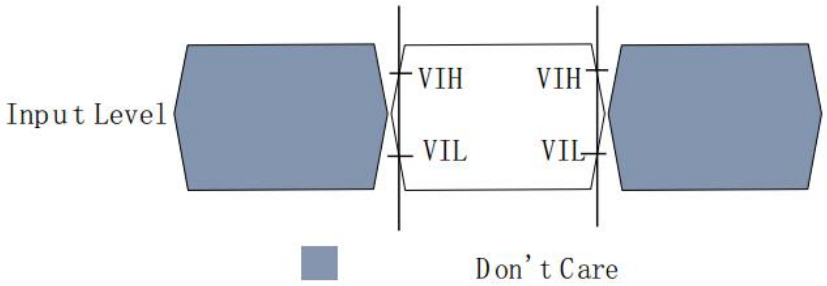


Figure 7 Input AC Timing Definitions for Reset_n and ODT_CA

7.1.2 AC Overshoot and Undershoot

Table 8 AC Overshoot and Undershoot for Address and Control Pins

Parameter	Specification
Maximum Allowed Peak Amplitude in Overshoot Region	0.35V
Maximum Peak Voltage Allowed in Undershoot Region	0.35V
Maximum Overshoot Region Above VDD/VDDQ	0.8V-ns

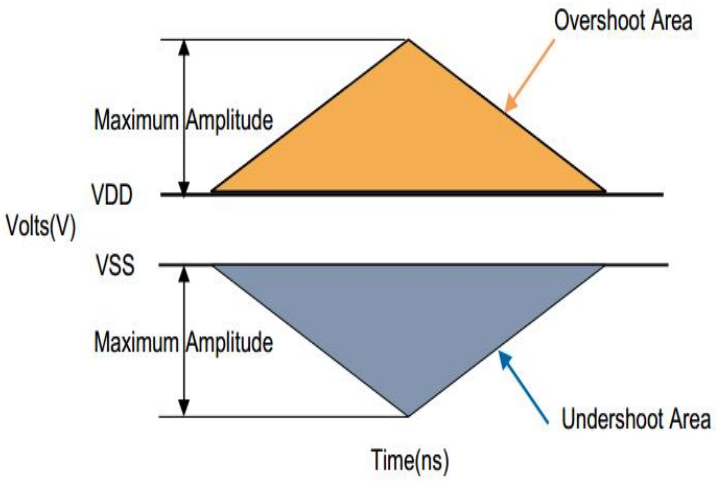


Figure 8 AC Overshoot and Undershoot for Address and Control Pins

7.2 Differential Input Voltage

The differential clock input levels must meet the specifications for Vindiff_CK and Vindiff_CK/2, measured over a single clock cycle. Vindiff_CK is the peak-to-peak voltage centered around 0V differential, and Vindiff_CK/2 is the maximum and minimum peak voltage relative to 0V.

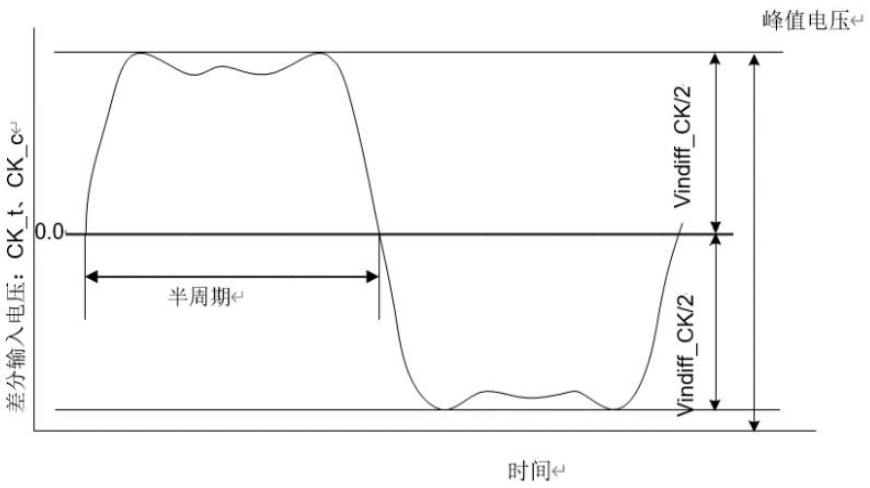


Figure 9 Differential Clock Input Levels

Table 14 Differential Clock Input Levels

Parameter	Symbol	Data Rate						Unit
		1600/1866		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Clock Input Voltage	Vindiff_CK	420	-	380	-	360	-	mV
a. The following requirements apply to all speed bins where DQ operating frequency is 1333 Mbps or lower; the first column is for 1600/1867.								
Note: 1. The peak-to-peak voltage of the differential CK signal is calculated by the following formula. 2. Vindiff_CK = (maximum peak voltage) - (minimum peak voltage) 3. Maximum peak voltage = V_peak_max 4. Minimum peak voltage = V_peak_min 5.f(t) = VCK_t - VCK_c								

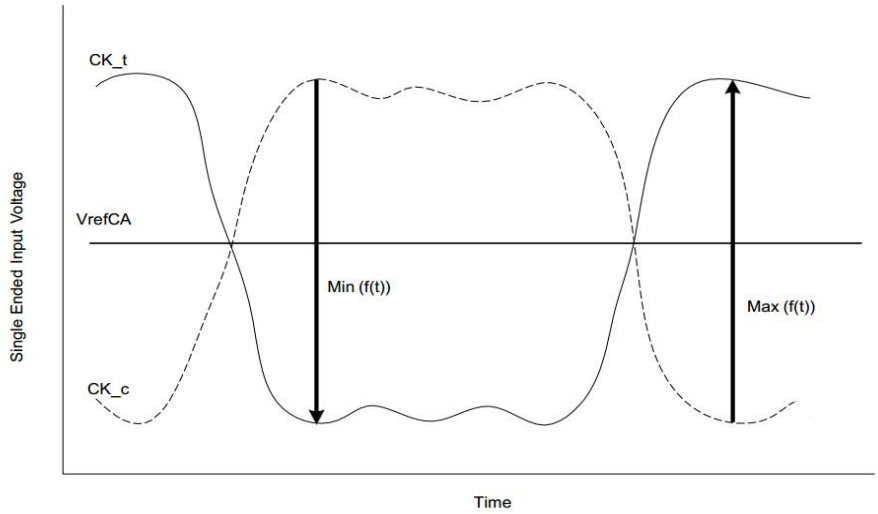


Figure 10 Differential Clock Peak-to-Peak Voltage

Note: VREFCA is an internal setting value obtained by the LPDDR4X SDRAM through VREF training.

7.3 Single-Ended Clock Input Levels

The single-ended clock input levels must simultaneously meet the specifications for V_se_CK, V_se_CK_High, and V_se_CK_Low.

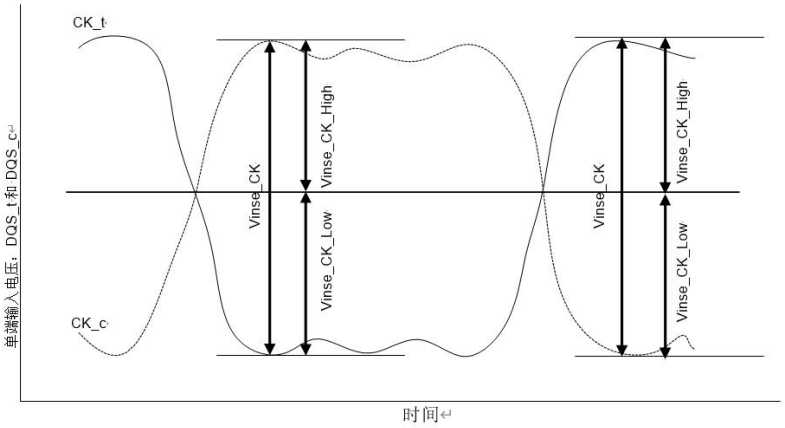


Figure 11 Single-Ended Clock Input Levels

Note: VREFCA is an internal setting value obtained by the LPDDR4X SDRAM through VREF training.

Table 10 Single-Ended Clock Input Levels

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Single-ended clock input voltage	Vinse_CK	210	-	190	-	180	-	mV
Single-ended clock input high voltage	Vinse_CK_High	105	-	95	-	90	-	mV
Single-ended clock input low voltage	Vinse_CK_Low	105	-	95	-	90	-	mV
a. The following requirements apply to all speed bins where DQ operating frequency is 1333 MT/s or lower; the first column is for 1600/1867.								

7.3.1 Clock Differential Clock Input Voltage Slew Rate

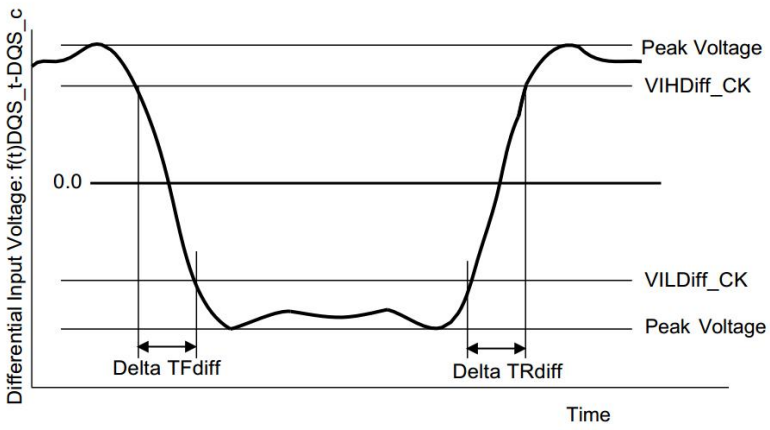


Figure 12 Differential Clock CK_t, CK_c Input Level Slew Rate

Note:

1. The rising edge of the differential signal from VILdiff_CK to VIHdiff_CK must have a monotonic slope.
2. The falling edge of the differential signal from VIHdiff_CK to VILdiff_CK must have a monotonic slope.

Table 16 CK_t, CK_c Input Level Slew Rate Definition

Description	Start Point	Trip Point	Definition
Differential Input Slew Rate for Rising Edge (CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	|VIHdiff_CK-VILdiff_CK|/DeltaTRdiff
Differential Input Slew Rate for Falling Edge (CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK-VIHdiff_CK|/DeltaTFdiff

Table 17 Differential Clock CK_t, CK_c Input Level Values

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input High Voltage	VIHdiff_CK	175	-	155	-	145	-	mV
Differential Input Low Voltage	VILdiff_CK	-	-175	-	-155	-	-145	mV
a. The following requirements apply to all speed bins with DQ operating frequencies of 1333 Mb/s and below; the values in the first column (1600/1867) also apply to these bins.								

Table 18 Differential Clock CK_t, CK_c Input Voltage Slew Rate

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input Clock Slew Rate	SRIdiff_CK	2	14	2	14	2	14	V/ns
a. The following requirements apply to all speed bins where DQ operating frequency is 1333 Mbps or lower; the first column is for 1600/1867.								

7.3.2 Differential Input Clock Cross Point Voltage

The differential input cross point voltage must meet the requirements shown in Figure 21. The measurement method for the differential input cross point voltage (VIX) is to measure the voltage at the cross point of the differential signals relative to the reference voltage VREFCA.

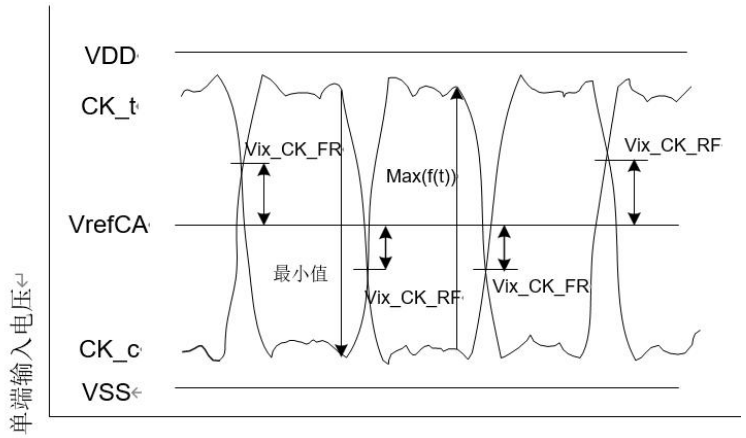


Figure 13 Definition of Differential Input Cross Point Voltage

Note: The reference level for Vix_CK_FR/RF is VREFCA, which is the internal setting value obtained through VREF training in LPDDR4X SDRAM.

Table 19 Differential Input Cross Point Voltage Values

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Clock Input Crossing Point Voltage Ratio1,2	Vix_CK_ratio	-	25	-	25	-	25	%
a. The following requirements apply to all speed bins with DQ operating frequency of 1333 MT/s or below; the first column is for 1600/1867.								
Note: 1. Vix_CK_Ratio is defined by the following formula: Vix_CK_Ratio = Vix_CK_FR / |Min(f(t))| 2. Vix_CK_Ratio is defined by the following formula: Vix_CK_Ratio = Vix_CK_RF / Max(f(t))								

7.3.3 DQS Differential Input Level

1) DQS differential input voltage level

The DQS differential input voltage level is denoted as Vindiff_DQS. Vindiff_DQS is the peak-to-peak voltage centered at 0V differential; Vindiff_DQS/2 is the maximum and minimum voltage swing relative to 0V.

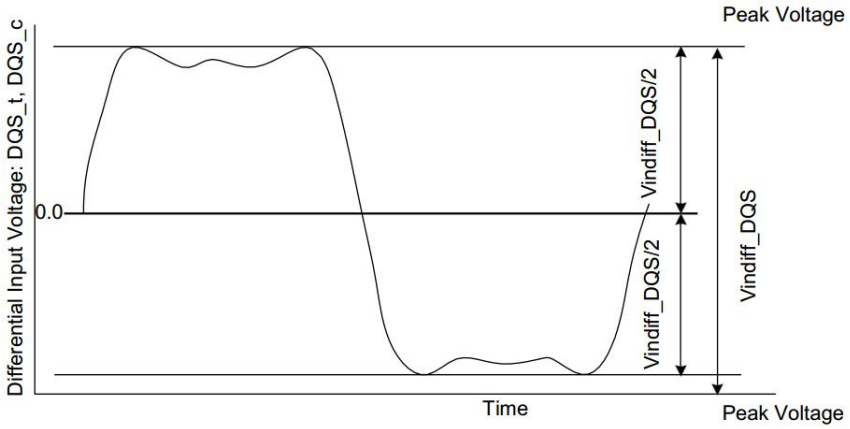


Figure 14 DQS Differential Input Voltage Level Diagram

Table 14 DQS Differential Input Voltage Level

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
DQS Differential Input [1]	Vindiff_DQS	360	-	360	-	340	-	mV
a. The following requirements apply to all speed bins where DQ operating frequency is 1333 Mbps or lower; the first column is for 1600/1867.								
Note: 1 The peak voltage of the differential DQS signal is calculated using the following formula.								

- Vindiff_DQS = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = Max(f(t))
- Minimum peak voltage = Min(f(t))

• f(t) = VDQS_t - VDQS_c

2) DQS peak voltage calculation method

The peak voltage of the differential DQS signal is calculated using the following equation:

- VIH.DIFF.Peak Voltage = Max(f(t))
- VIL.DIFF.Peak Voltage = Min(f(t))
- f(t) = VDQS_t - VDQS_c

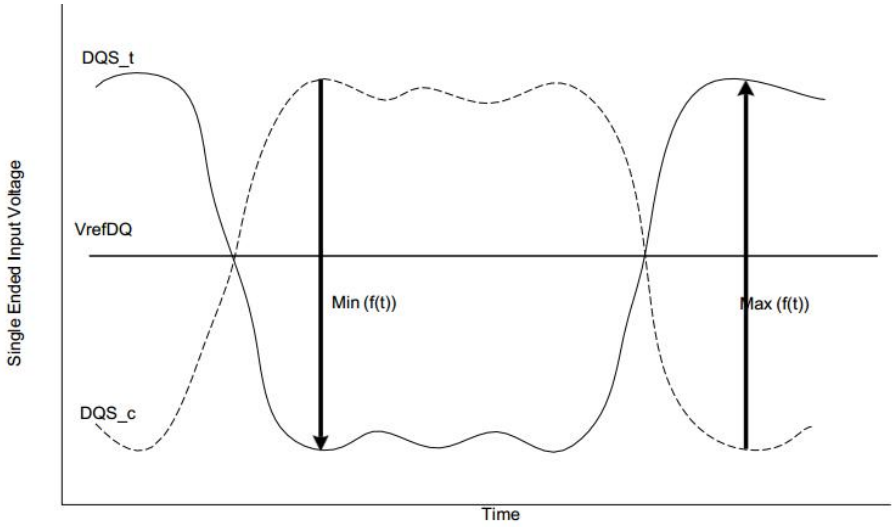


Figure 15 Definition of differential DQS peak voltage

Note: VrefDQ is an internal setting value obtained by the LPDDR4X SDRAM through Vref training.

7.3.4 DQS Single-Ended Input Level

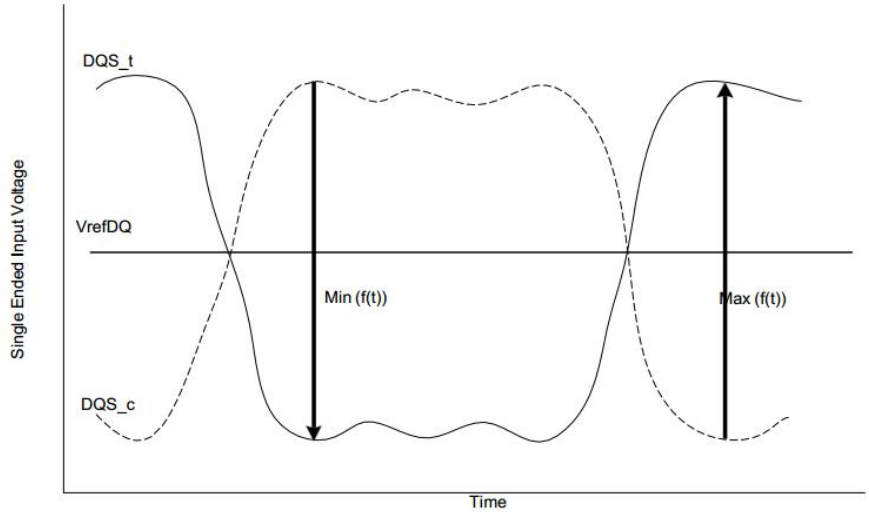


Figure 16 DQS Single-Ended Input Voltage Diagram

Note: VrefDQ is an internal setting value obtained by the LPDDR4X SDRAM through Vref training.

Table 21 DQS Single-Ended Input Level

Parameter	Symbol	Data Rate			Unit
		1600/1867[a]	2133/2400/3200	3733/4266	

		Min	Max	Min	Max	Min	Max	
DQS differential input voltage	Vindiff_DQS	180	-	180	-	170	-	mV
DQS Single-Ended Input High Voltage	VIH(se)_DQS	90	-	90	-	85	-	mV
VIL_DQS (DQS Single-Ended Input Low Voltage)	VIL(se)_DQS	90	-	90	-	85	-	mV
a. The following requirements apply to all speed bins where DQ operating frequency is 1333 Mbps or lower; the first column is for 1600/1867.								

7.3.5 DQS Differential Input Voltage Slew Rate

The definition and measurement of the differential signal (DQS_t, DQS_c) input voltage slew rate are shown in the following figure.

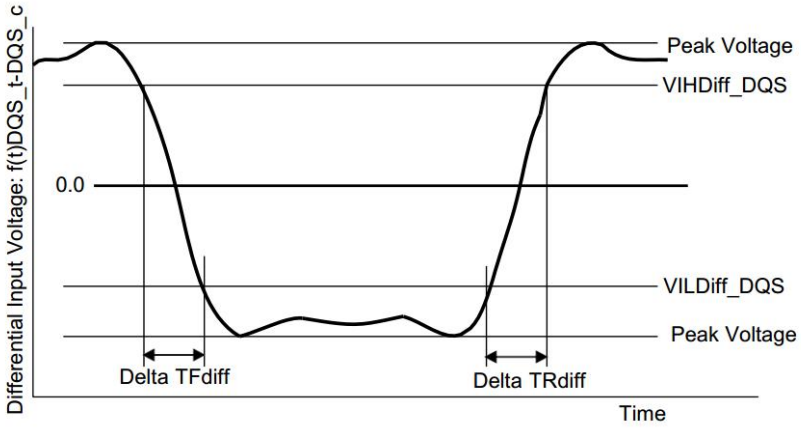


Figure 17 DQS_t, DQS_c Input Voltage Slew Rate Diagram

Note:

1. The rising edge of the differential signal from VILdiff_DQS to VIHdiff_DQS must have a monotonic slope.

2. The differential falling edge from VIHdiff_DQS to VILdiff_DQS must have a monotonic slope.

Table 22 DQS_t, DQS_c Input Slew Rate Definition

Description	Measurement Point	Trip Point	Definition
Differential Input Slew Rate for Rising Edge	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTRdiff
Differential Input Slew Rate for Falling Edge	VIHdiff_DQS	VILdiff_DQS	|VIHdiff_DQS - VILdiff_DQS|/DeltaTFdiff

Table 23 DQS_t, DQS_c Input Level Reference Values

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	

Differential Input High Level	VIHdiff_DQS	140	-	140	-	120	-	mV
Differential Input Low Level	VILdiff_DQS	-	-140	-	-140	-	-120	mV
a. The following requirements apply to all speed bins where DQ operating frequency is 1333 Mbps or lower; the first column is for 1600/1867.								

Table 24 DQS_t, DQS_c Differential Input Voltage Slew Rate Reference Values

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input Slew Rate	SRIdiff	2	14	2	14	2	14	V/ns

7.3.6 DQS Differential Input Cross Point Voltage

The differential input signals for DQS are DQS_t and DQS_c. The differential input cross point voltage VIX is measured as the voltage at the cross point of the differential levels with respect to the reference voltage VREFDQ.

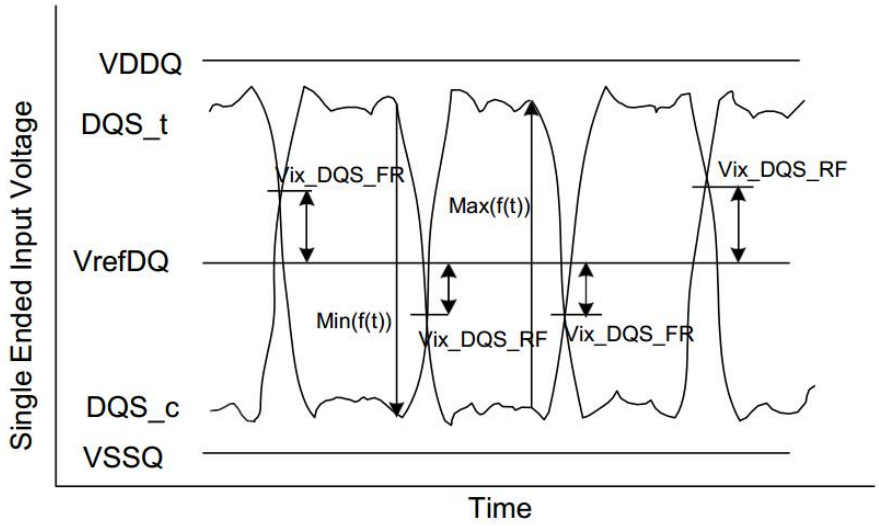


Figure 18 Vix Definition of DQS

Note: The reference level for Vix_DQS_FR/RF is VrefDQ, which is the internal set value obtained by LPDDR4X SDRAM through Vref training.

Table 25 Differential Input Cross Point Voltage for DQS

Parameter	Symbol	Data Rate						Unit
		1600/1867[a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
DQS Differential Input Cross-Point Voltage Ratio1,2	Vix_DQS_ratio	-	20	-	20	-	20	%
a. The following requirements apply to all speed bins with DQ operating frequency ≤ 1333 MT/s; the first column is 1600/1867.								
Note:								
1. Vix_DQS_Ratio is defined by: Vix_DQS_Ratio = Vix_DQS_FR / |Min(f(t))|.								

2. Vix_DQS_Ratio is defined by: Vix_DQS_Ratio = Vix_DQS_RF / Max(f(t)).

7.4 ODT Input AC/DC Input Levels

Table 26 ODT Input Levels

Parameter	Symbol	Min	Max	Unit
ODT Input High Level (AC)	VIHODT (AC)	0.75*VDD	VDD+0.2	V
VILODT (AC)	VILODT(AC)	-0.2	0.25*VDD	V
VIHODT (DC)	VIHODT(DC)	0.65*VDD	VDD+0.2	V
VILODT (DC)	VILODT (DC)	-0.2	0.35*VDD	V
Note:				
See overshoot and undershoot specifications.				

7.5 LVSTL Overshoot and Undershoot

Table 27 AC Overshoot/Undershoot Specifications

Parameter	Min/Max	Data Rate		Unit
		1600/1866/3200	4266	
Maximum Allowed Peak Amplitude in Overshoot Region	Max	0.3	TBD	V
Maximum undershoot peak amplitude	Max	0.3	TBD	V
Maximum area above VDD	Max	0.1	TBD	V/ns
Maximum area below VSS	Max	0.1	TBD	V/ns
Note:				
1. VDD2 is the supply voltage for CA[5:0], CK_t, CK_c, CS_n, CKE, and ODT; VDDQ is the supply voltage for DQ, DMI, DQS_t, and DQS_c.				
2. VSS is the reference ground for CA[5:0], CK_t, CK_c, CS_n, CKE, and ODT; VSSQ is the reference ground for DQ, DMI, DQS_t, and DQS_c.				
3. Maximum peak amplitude values are referenced to the actual VDD and VSS values.				
4. Maximum area values are referenced to the maximum operating VDD and VSS values.				

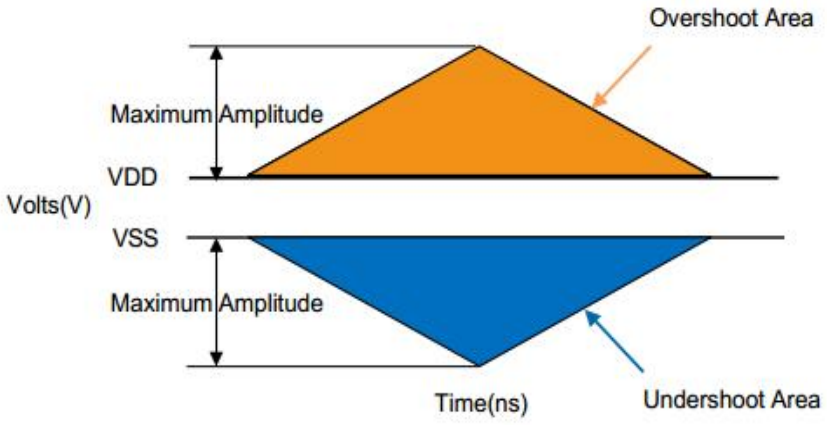


Figure 19 Overshoot and Undershoot Definitions

7.6 Driver Output Timing Reference Load

During circuit design, IBIS or other simulation tools should be used to correlate the timing reference load with the system environment.

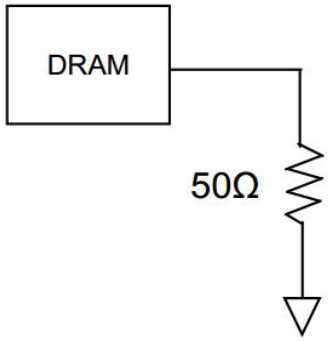


Figure 20 Output Timing Reference Load

7.7 LVSTL (Low Voltage Swing Terminated Logic) I/O System

The LVSTL I/O cell consists of a pull-up driver, a pull-down driver, and a terminator. The basic cell is shown in the figure below:

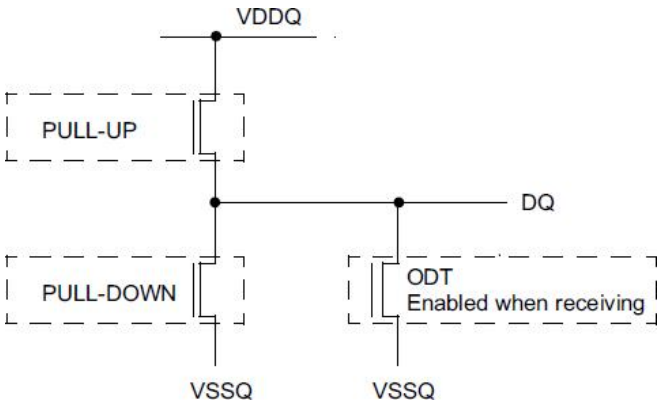


Figure 21 LVSTL I/O Cell Structure

To ensure the target impedance is achieved, the LVSTL I/O cell is designed to be calibrated. The steps are as follows:

- First, calibrate the pull-down device, which is connected to VDDQ through the ZQ pin and a 240 Ω resistor.
- Set the drive strength control to the minimum value.
- Increase the drive strength until the comparator detects that the ZQ pin voltage is less than VDDQ/2.
- The NMOS pull-down device is calibrated to 240 Ω.

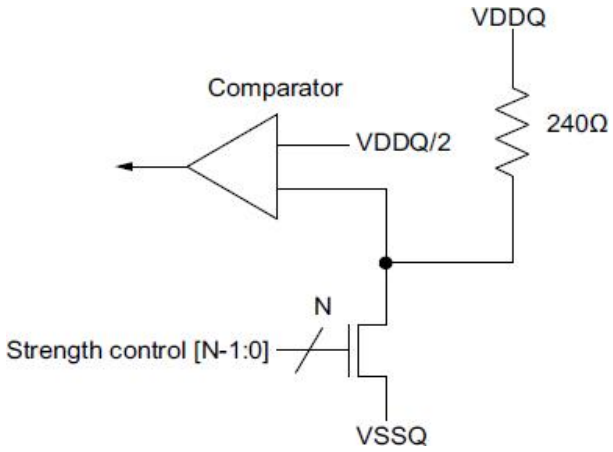
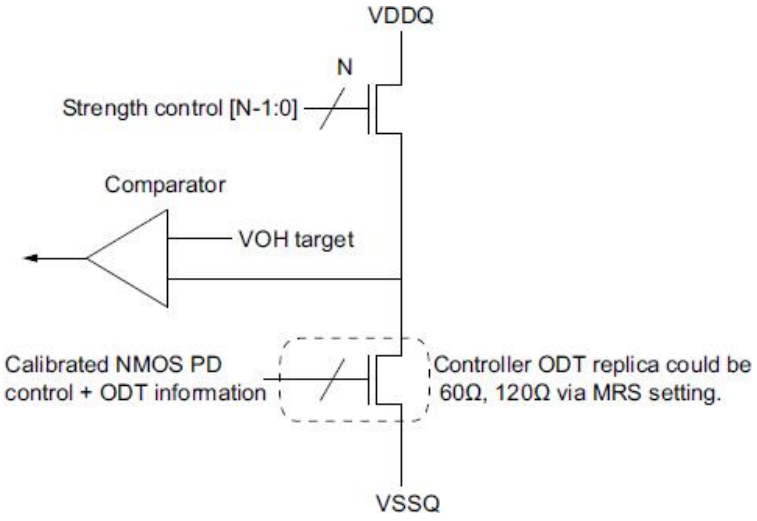


Figure 22 Pull-Down Calibration

Then calibrate the pull-up device based on the calibrated pull-down device.

- Set the VOH target via MRS and configure the ODT of the NMOS controller (VOH can be automatically controlled by ODT MRS).
- Set the drive strength control to the minimum value.
- Increase the drive strength until the comparator detects that the data bit is greater than the VOH target value.
- NMOS pull-up device is now calibrated to the VOH target value.

Figure 23 Pull-Up Calibration



8. Input/Output Capacitance

Table 28 Input/Output Capacitance

Parameter	Symbol	Min/Max	3200 - 533	4266-3733	Unit	Remarks
Input capacitance, CK_t and CK_c	CCK	Min	0.5	TBD	pF	1,2
		Max	0.9	TBD		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0	TBD	pF	1,2,3
		Max	0.09	TBD		
Input capacitance,	C_I	Min	0.5	TBD	pF	1,2,4

all other input-only pins		Max	0.9	TBD		
Input capacitance delta, all other pure input pins	CDI	Min	-0.1	TBD	pF	1,2,5
		Max	0.1	TBD		
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	Min	0.7	TBD	pF	1,2,6
		Max	1.3	TBD		
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	0	TBD	pF	1,2,7
		Max	0.1	TBD		
Input/output capacitance delta, DQ, DMI	CDIO	Min	-0.1	TBD	pF	1,2,8
		Max	0.1	TBD		
Input/Output capacitance, ZQ pin	CZQ	Min	0	TBD	pF	1,2
		Max	5	TBD		

Note:

1. This parameter applies only to the die device (excluding package capacitance).
2. This parameter is not production tested. It is ensured through design and characterization. Capacitance is measured per JEP147 (procedure for measuring input capacitance using a vector network analyzer (VNA)) with VDD1, VDD2, VDDQ, VSS, VSSQ at operating conditions and all other pins floating.
3. Absolute value of CCK_t. CCK_c.
4. CI applies to CS_n, CKE, CA0–CA5.
5. CDI = CI .0.5× (CCK_t + CCK_c).
6. DMI loading matches DQ and DQS.
7. Absolute values of CDQS_t and CDQS_c.
8. CDIO = CIO + 0.5 × (CDQS_t + CDQS_c) per byte lane.

9. IDD Test Conditions and Specifications

9.1 IDD Measurement Conditions

Unless otherwise noted, the following definitions apply in the IDD measurement tables:

Low: VIN ≤ VIL(DC) max

High: VIN ≥ VIH(DC) min

Stable: Inputs are stable at a high or low level

Switching: See Table 32 and Table 33

Table 29 Input Signal Switching Definitions

CA Transition								
CK_t Edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	High	High	High	High	High	High	High	High
CS	Low	Low	Low	Low	Low	Low	Low	Low
CA0	High	Low	Low	Low	Low	High	High	High
CA1	High	High	High	Low	Low	Low	Low	High
CA2	High	Low	Low	Low	Low	High	High	High

CA3	High	High	High	Low	Low	Low	Low	High
CA4	High	Low	Low	Low	Low	High	High	High
CA5	High	High	High	Low	Low	Low	Low	High
Note:								
1. CS must always be Low.								
2. 50% of the CA bus toggles between High and Low, changing once per clock.								
3. For IDD values requiring CA bus toggling, this pattern is used continuously during IDD measurements.								

Table 30 CA Pattern for IDD4R

Clock Cycles	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	High	High	Read-1	L	H	L	L	L	L
N+1	High	Low		L	H	L	L	L	L
N+2	High	High	CAS-2	L	H	L	L	H	L
N+3	High	Low		L	L	L	L	L	L
N+4	High	Low	DES	L	L	L	L	L	L
N+5	High	Low	DES	L	L	L	L	L	L
N+6	High	Low	DES	L	L	L	L	L	L
N+7	High	Low	DES	L	L	L	L	L	L
N+8	High	High	Read-1	L	L	L	L	L	L
N+9	High	Low		L	L	L	L	L	L
N+10	High	High	CAS-2	L	H	L	L	H	H
N+11	High	Low		H	H	H	H	H	H
N+12	High	Low	DES	L	L	L	L	L	L
N+13	High	Low	DES	L	L	L	L	L	L
N+14	High	Low	DES	L	L	L	L	L	L
N+15	High	Low	DES	L	L	L	L	L	L
Note:									
1BA[2:0] = 010, CA[9:4] = 000000 or 111111, burst order CA[3:2] = 00 or 11 (same as LPDDR3 IDD4R).									
2Different from LPDDR3 (JESD209-3): CA pins remain Low during DES command to reduce ODT current.									

Table 31 CA Pattern for IDD4W

Clock Cycles	CKE	CS	Common Task	CA0	CA1	CA2	CA3	CA4	CA5
N	High	High	Write-1	L	L	H	L	L	L
N+1	High	Low		L	H	L	L	L	L
N+2	High	High	CAS-2	L	H	L	L	H	L
N+3	High	Low		L	L	L	L	L	L
N+4	High	Low	DES	L	L	L	L	L	L
N+5	High	Low	DES	L	L	L	L	L	L
N+6	High	Low	DES	L	L	L	L	L	L
N+7	High	Low	DES	L	L	L	L	L	L
N+8	High	High	Write-1	L	L	H	L	L	L
N+9	High	Low		L	H	L	L	H	L
N+10	High	High	CAS-2	L	H	L	L	H	H
N+11	High	Low		L	L	H	H	H	H

N+12	High	Low	DES	L	L	L	L	L	L
N+13	High	Low	DES	L	L	L	L	L	L
N+14	High	Low	DES	L	L	L	L	L	L
N+15	High	Low	DES	L	L	L	L	L	L
Note: 1BA[2:0] = 010, CA[9:4] = 000000 or 111111 (same as LPDDR3 IDD4W).									

Table 32 IDD4W Data Pattern (DBI Off)

DBI Off Case										No. of1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No.of1s	16	16	16	16	16	16	16	16		
Note:										
Compared with the previous generation, the data pattern is simplified. DQ[4], DQ[5], DQ[6], and DQ[7] use the same data pattern to reduce the complexity of IDD4W/R programming.										

Table 33 IDD4R Data Pattern (DBI Off)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	No. of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	1	1	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of1s	16	16	16	16	16	16	16	16	16	
Note:										
The same data pattern is applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce the complexity of IDD4W/R programming.										

Table 34 IDD4W Data Pattern (DBI On)

DBI ON Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	No. of1s
BL0	0	0	0	0	0	0	0	0	1	1

BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	0	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	0	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	0	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	0	0	0	0	1	1	1	1	0	4
No. of1s	8	8	8	8	8	8	16	16	8	
Note:										
Burst with DBI enabled.										

Table 35 IDD4R Data Pattern (DBI On)

DBI ON Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	No. of1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4

BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	0	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	0	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	0	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	0	0	0	0	1	1	1	1	0	4
No. of1s	8	8	8	8	8	8	16	16	8	

9.2 IDD Parameters

IDD values apply over the full operating voltage range and over the full temperature range, except IDD6ET which applies over the full high-temperature range.

Table 36 IDD Specifications and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Remarks
Operating one-bank activate-precharge current: tCK = tCK(min); tRC = tRC(min); CKE high; CS low between valid commands; CA bus inputs switching; data bus inputs stable, ODT disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK = tCK(min); CKE low; CS low; all banks idle; CA bus inputs switching; data bus inputs stable, ODT disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Standby idle power-down current with clock stop: CK_t = Low, CK_c = High; CKE	IDD2PS1	VDD1	

= Low; CS = Low; all banks idle; CA bus inputs static; data bus inputs static; ODT disabled	IDD2PS2	VDD2	
	IDD2PSQ	VDDQ	3
Standby idle non-power-down current: tCK = tCKmin; CKE = High; CS = Low; all banks idle; CA bus inputs switching; data bus inputs static; ODT disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Standby idle non-power-down current with clock stop: CK_t = Low, CK_c = High; CKE = High; CS = Low; all banks idle; CA bus inputs static; data bus inputs static; ODT disabled	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NSQ	VDDQ	3
Active power-down standby current: tCK = tCKmin; CKE = Low; CS = Low; one bank active; CA bus inputs switching; data bus inputs static; ODT disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stop: CK_t = Low, CK_c = High; CKE = Low; CS = Low; one bank active; CA bus inputs static; data bus inputs static; ODT disabled	IDD3PS1	VDD1	
	IDD3PS2	VDD2	
	IDD3PSQ	VDDQ	4
Active non-power-down standby current: tCK = tCKmin; CKE = High; CS = Low; one bank active; CA bus inputs switching; data bus inputs static; ODT disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stop: CK_t = Low, CK_c = High; CKE = High; CS = Low; one bank active; CA bus inputs static; data bus inputs static; ODT disabled	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Burst mode read current: tCK = tCKmin; CS = Low between valid commands; one bank active; BL = 16 or 32; RL = RL(MIN); CA bus inputs switching; 50% data change per burst transfer; ODT disabled	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Burst write current: tCK = tCKmin; CS is Low between valid commands; one bank active; BL = 16 or 32; WL = WLmin; CA bus inputs toggling; 50% data change per burst transfer; ODT disabled	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All bank refresh burst current: tCK = tCKmin; CKE is High between valid commands; tRC = tRFCabmin; burst refresh; CA bus inputs toggling; data bus inputs stable; ODT disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4
All bank REFRESH average current: tCK = tCKmin; CKE is High between valid commands; tRC = tREFI; CA bus inputs toggling; data bus inputs stable; ODT disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5ABQ	VDDQ	4
Per bank REFRESH average current: tCK = tCKmin; CKE is High between valid commands; tRC = tREFI/8; CA bus inputs toggling; data bus inputs stable; ODT	IDD5PB1	VDD1	
	IDD5PB2	VDD2	

disabled	IDD5PBQ	VDDQ	4
Power-down self-refresh current (-25°C to +85°C): CK_t = Low, CK_c = High; CKE is Low; CA bus inputs stable; data bus inputs stable; maximum 1x self-refresh rate; ODT disabled	IDD61	VDD1	6,7,8,10
	IDD62	VDD2	6,7,8,10
	IDD6Q	VDDQ	4,6,7,8,10
Power-down self-refresh current (+85°C to +105°C): CK_t = Low, CK_c = High; CKE is Low; CA bus inputs stable; data bus inputs stable; maximum 1x self-refresh rate; ODT disabled	IDD6ET1	VDD1	7,8,11
	IDD6ET2	VDD2	7,8,11
	IDD6ETQ	VDDQ	4,7,8,11
Note:			
1. With DBI enabled, the IDD value is the maximum of the arithmetic mean distribution.			
2. ODT disabled: MR11[2:0]=000B.			
3. IDD current specifications are tested after proper device initialization.			
4. Measured current is the sum of VDDQ and VDD2.			
5. Design guaranteed with output load = 5 pF and RON = 40 Ω.			
6. 1x self-refresh rate is the rate at which LPDDR4X devices perform internal refresh during self-refresh before entering the high temperature range.			
7. This is the general definition applicable to full array self refresh.			
8. Supplier datasheets may include additional self refresh IDD values for temperature sub-ranges within the standard or extended temperature range.			
9. In all IDD measurements, VIHCKE = 0.8×VDD2, VILCKE = 0.2×VDD2.			
10. IDD6 at 85°C is guaranteed; IDD6 at 45°C is typical (arithmetic mean distribution).			
11. IDD6ET is typical, sample value only, not tested.			
12. Dual-channel devices are specified for dual-channel operation (both channels running simultaneously).			

9.3 LPDDR4X IDD Parameters – Single Die

VDD2=1.06~1.17V,VDDQ=1.06~1.17V;VDD1=1.70~1.95V;TC =-40℃~+85℃;

Table 37 LPDDR4X IDD Parameters – Single Die

Symbol	Power Supply	4266Mbps	Unit
$IDD0_1$	VDD1	2.6	mA
$IDD0_2$	VDD2	41.5	
IDD0Q	VDDQ	1.2	
$IDD2P_1$	VDD1	0.3	mA
$IDD2P_2$	VDD2	1.2	
IDD2PQ	VDDQ	1.2	
$IDD2PS_1$	VDD1	0.5	mA
$IDD2PS_2$	VDD2	2.3	
IDD2PSQ	VDDQ	1.2	
$IDD2N_1$	VDD1	0.5	mA
$IDD2N_2$	VDD2	20.8	

IDD2NQ	VDDQ	1.2	
$IDD2NS_1$	VDD1	0.5	mA
$IDD2NS_2$	VDD2	15.1	
IDD2NSQ	VDDQ	1.2	
$IDD3P_1$	VDD1	0.7	mA
$IDD3P_2$	VDD2	8.4	
IDD3PQ	VDDQ	1.2	
$IDD3PS_1$	VDD1	0.7	mA
$IDD3PS_2$	VDD2	8.4	
IDD3PSQ	VDDQ	1.2	
$IDD3N_1$	VDD1	1.1	mA
$IDD3N_2$	VDD2	26.7	
IDD3NQ	VDDQ	1.2	
$IDD3NS_1$	VDD1	1.1	mA
$IDD3NS_2$	VDD2	21	
IDD3NSQ	VDDQ	1.2	
$IDD4R_1$	VDD1	4	mA
$IDD4R_2$	VDD2	284.2	
IDD4RQ	VDDQ	91.9	
$IDD4W_1$	VDD1	3.5	mA
$IDD4W_2$	VDD2	235.2	
IDD4WQ	VDDQ	1.2	
$IDD5_1$	VDD1	9.9	mA
$IDD5_2$	VDD2	105.4	
IDD5Q	VDDQ	1.2	
$IDD5AB_1$	VDD1	1.2	mA
$IDD5AB_2$	VDD2	26.3	
IDD5ABQ	VDDQ	1.2	
$IDD5PB_1$	VDD1	1.3	mA
$IDD5PB_2$	VDD2	26.7	
IDD5PBQ	VDDQ	1.2	

9.4 LPDDR4X IDD6 Parameters - Single Die

VDD2=1.06~1.17V,VDDQ=1.06~1.17V;VDD1=1.70~1.95V;TC =-40℃~+85℃;

Table 38 LPDDR4X IDD6 Parameters - Single Die

Temperature	Symbol	Power Supply	Full Array Self-Refresh Current	Unit
25℃	$IDD6_1$	V_{DD1}	0.6	mA
	$IDD6_2$	V_{DD2}	3.3	

	IDD6Q	V_{DDQ}	0.1	
85℃	$IDD6_1$	V_{DD1}	0.8	mA
	$IDD6_2$	V_{DD2}	5.2	
	IDD6Q	V_{DDQ}	0.1	

9.5 LPDDR4X IDD Parameters - Single Die

VDD2=1.06~1.17V,VDDQ=0.57~0.65V;

VDD1=1.70~1.95V,TC=-40℃~ +85℃;

Table 39 LPDDR4X IDD Parameters - Single Die

Symbol	Power Supply	4266Mbps	Unit
IDD01	V_{DD1}	2.6	mA
IDD02	V_{DD2}	41.5	
IDD0Q	V_{DDQ}	1.2	
IDD2P1	V_{DD1}	0.3	mA
IDD2P2	V_{DD2}	1.2	
IDD2PQ	V_{DDQ}	1.2	
$IDD2PS_1$	V_{DD1}	0.5	mA
$IDD2PS_2$	V_{DD2}	2.3	
IDD2PSQ	V_{DDQ}	1.2	
$IDD2N_1$	V_{DD1}	0.5	mA
$IDD2N_2$	V_{DD2}	20.8	
IDD2NQ	V_{DDQ}	1.2	
IDD2NS1	V_{DD1}	0.5	mA
IDD2NS2	V_{DD2}	15.1	
IDD2NSQ	V_{DDQ}	1.2	
IDD3P1	V_{DD1}	0.7	mA
IDD3P2	V_{DD2}	8.4	
IDD3PQ	V_{DDQ}	1.2	
$IDD3PS_1$	V_{DD1}	0.7	mA
$IDD3PS_2$	V_{DD2}	8.4	
IDD3PSQ	V_{DDQ}	1.2	
$IDD3N_1$	V_{DD1}	1.1	mA
$IDD3N_2$	V_{DD2}	26.7	
IDD3NQ	V_{DDQ}	1.2	
$IDD3NS_1$	V_{DD1}	1.1	mA

$IDD3NS_2$	V_{DD2}	21	
IDD3NSQ	V_{DDQ}	1.2	
$IDD4R_1$	V_{DD1}	4	
$IDD4R_2$	V_{DD2}	284.2	mA
IDD4RQ	V_{DDQ}	91.9	
$IDD4W_1$	V_{DD1}	3.5	
IDD4W2	V_{DD2}	235.2	mA
IDD4WQ	VDDQ	1.20	
IDD51	VDD1	9.9	
IDD52	VDD2	105.4	mA
IDD5Q	V_{DDQ}	1.20	
IDD5AB1	V_{DD1}	1.2	
IDD5AB2	V_{DD2}	26.3	mA
IDD5ABQ	V_{DDQ}	1.20	
IDD5PB1	V_{DD1}	1.3	
IDD5PB2	V_{DD2}	26.7	mA
IDD5PBQ	V_{DDQ}	1.20	

9.6 LPDDR4X IDD6 Parameters - Single Die

VDD2=1.06~1.17V,VDDQ=0.57~0.65V;

VDD1=1.70~1.95V,TC=-40℃~ +85℃;

Table 40 LPDDR4X IDD6 Parameters - Single Die

Operating Temperature	Symbol	Power Supply	Full Array Self-Refresh Current	Unit
25℃	$IDD6_1$	V_{DD1}	0.6	mA
	$IDD6_2$	V_{DD2}	3.3	
	IDD6Q	V_{DDQ}	0.1	
85℃	$IDD6_1$	V_{DD1}	0.8	mA
	$IDD6_2$	V_{DD2}	5.2	
	IDD6Q	V_{DDQ}	0.1	

10. Electrical Characteristics and AC Timing

10.1 Clock Characteristics

10.1.1 Definition of tCK(avg) and nCK

tCK(avg) is calculated as the average clock period over any consecutive window of 200 cycles, where each clock period is measured from rising edge to rising edge.

$$tCK(avg) = \left| \sum_{j=1}^{N} tCK_j \right| /N \quad N=200$$

The unit "tCK(avg)" represents the actual average clock period tCK(avg) of the input clock in operation. The unit "nCK" represents one clock cycle of the input clock, counting actual clock edges. The variation of tCK(avg) over a window of 200 clock cycles can be up to +/-1%, provided all jitter and timing specifications are met.

10.1.2 Definition of tCK(abs)

tCK(abs) is defined as the absolute clock period measured from one rising edge to the next consecutive rising edge.

1) Definition of tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width over 200 consecutive high pulses.

$$tCH(avg) = \left| \sum_{j=1}^{N} tCHj \right| / \{N \times tCK(avg)\} \quad N=200$$

tCL(avg) is defined as the average low pulse width over 200 consecutive low pulses.

$$tCL(avg) = \left| \sum_{j=1}^{N} tCLj \right| / \{N \times tCK(avg)\} \quad N=200$$

2) Definition of tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, measured from a rising edge to the next falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, measured from a falling edge to the next rising edge.

3) Definition of tJIT(per)

tJIT(per) is the per-cycle jitter, defined as the maximum deviation of any signal tCK from tCK(avg).

tJIT(per) is the minimum/maximum value of {tCK_i - tCK(avg)} where i = 1 to 200. tJIT(per),act is the actual clock jitter for a given system.

4) Definition of tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles. tJIT(cc) is the maximum value of |tCK(i+1) - tCK(i)|.

tJIT(cc) defines cycle-to-cycle jitter.

10.2 Clock Timing

Table 31 Clock AC Timing

Parameter	Symbol	1600/2400/3200		Unit
		Min	Max	
Clock cycle time				
Average high pulse width	tCH (average)	0.46	0.54	tCK (avg)

Average Low Pulse Width	tCL (average)	0.46						0.54		tCK (avg)
Absolute Clock Period	tCK(abs)	tCK (avg) min + tJIT (per) min						-		ns
Absolute High Level Clock Pulse Width	tCH(abs)	0.43						0.57		tCK (avg)
Absolute Low Clock Pulse Width	tCL(abs)	0.43						0.57		tCK (avg)
Parameter	Symbol	1600		2400		3200		4266		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Timing										
Average Clock Period	tCK (avg)	1.25	100	0.833	100	0.625	100	0.468	100	ns
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps
Cycle-to-cycle jitter Between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps

10.3 AC Timing Temperature Derating

Table 42 Temperature Derating AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/ 2667/3200/3733/4267	
DQS output access time from CK_t/CK_c (derated)	tDQSCK	Min	3600	ps
RAS to CAS delay (derated)	tRCD	Min	tRCD + 1.875	ns
ACTIVATE to ACTIVATE Command Period (Derated)	tRC	Min	tRC + 3.75	ns
Row Active Time (Derated)	tRAS	Min	tRAS + 1.875	ns
Row Precharge Time (Derated)	tRP	Min	tRP + 1.875	ns
Active Group A to Active Group B (Derated)	tRRD	Min	tRRD + 1.875	ns
Note: Timing derating applies to operation at temperatures from 85°C to 105°C.				

10.4 CA Receiver Voltage and Timing

The figure below shows the compliance mask for command and address (CA), including CS input receiver voltage and timing. All CA and CS signals apply the same compliance mask and operate in single data rate mode. The receiver mask (Rx mask) defines the region where input signals must not interfere, so that the DRAM input receiver can correctly capture valid input signals.

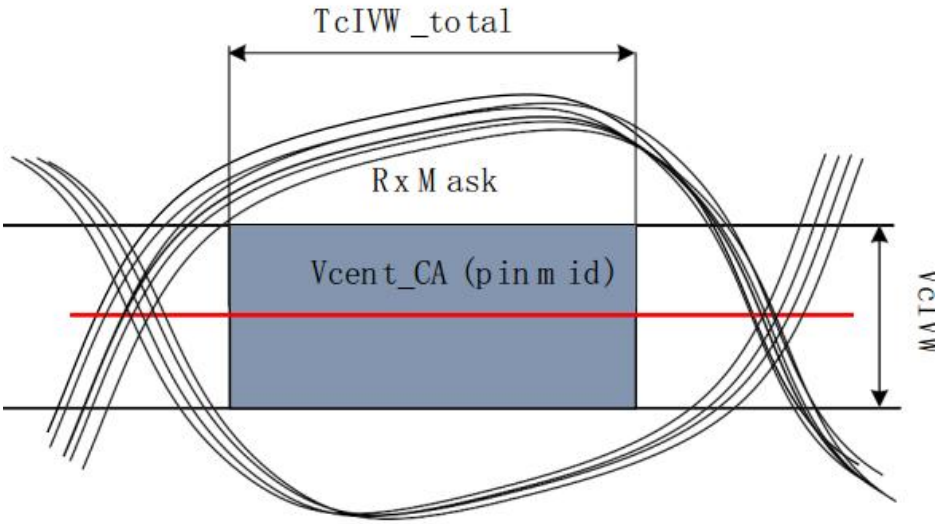


Figure 24 CA Receiver (RX) Schematic

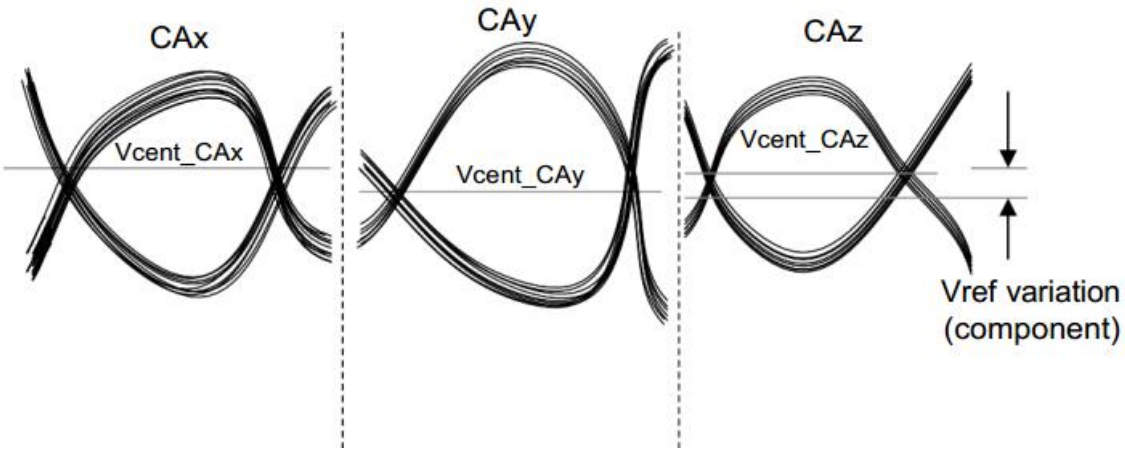


Figure 25 Cross-Pin VREFCA Voltage Variation

Vcent_CA (pin midpoint) is defined as the midpoint between the maximum and minimum Vcent_CA voltage levels across all CA and CS pins of a given DRAM component. As shown in Figure 25, each CA Vcent level is defined by the center of the cumulative data input eye (i.e., the widest opening). This indicates that the level variation of any DRAM must be considered in the DRAM CA Rx mask. VREF will be set by the system for Ron and ODT settings.

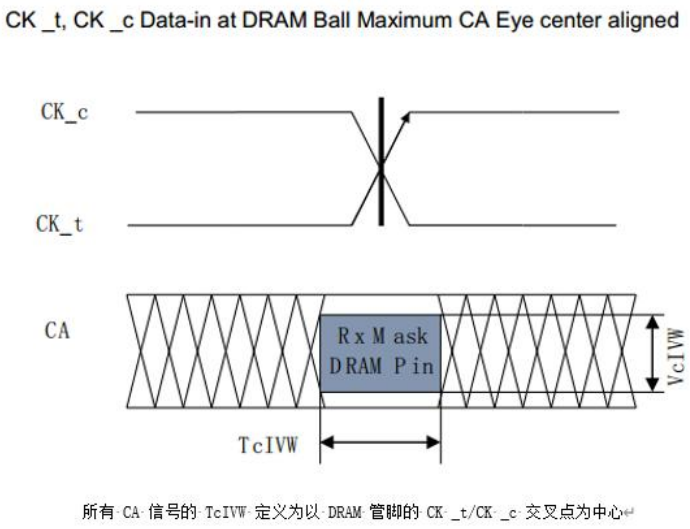


Figure 26 DRAM Pin CA Timing

All timing parameters in Figure 26 are measured from CK_t/CK_c to the center (midpoint) of the tCIVW window, which is taken from the VcIVW_total voltage centered at Vcent_CA (pin midpoint).

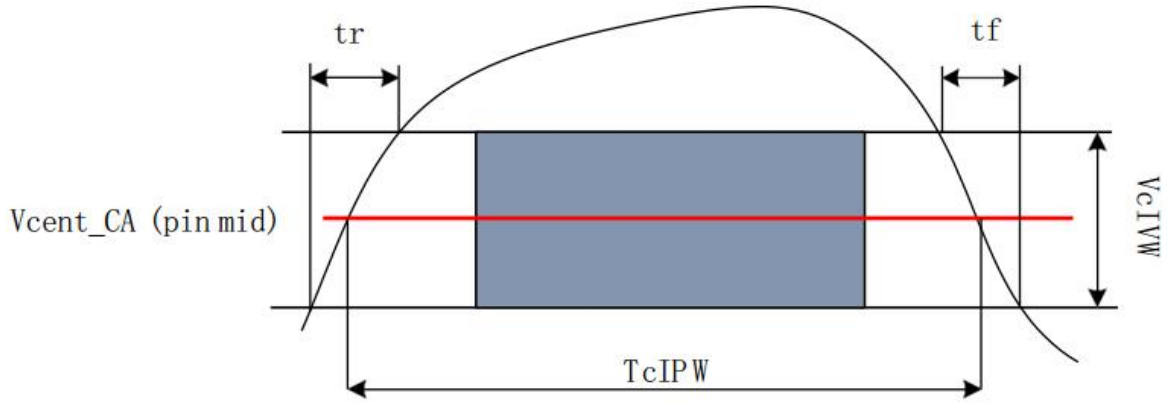


Figure 27 CA tCIPW and SRIN_cIVW Definition (for each input pulse)

Note: SRIN_cIVW = VcIVW_Total / (tr or tf), the signal must be monotonic within tr and tf range.

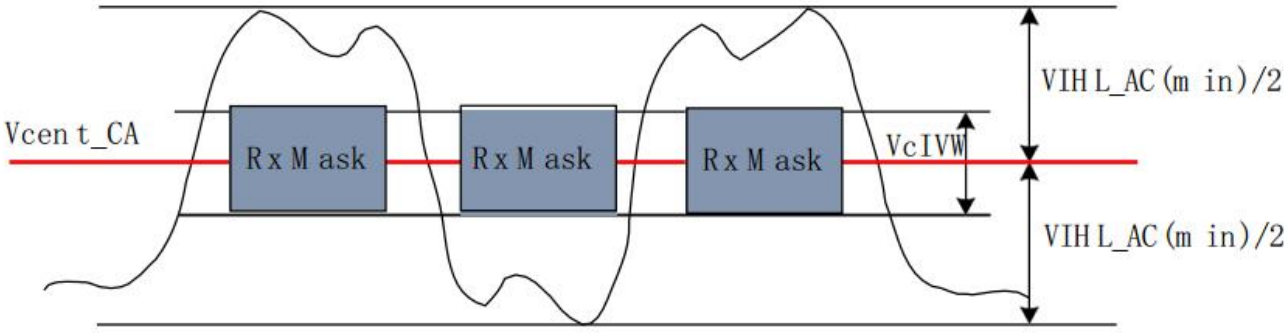


Figure 28 CA VIHL(AC) Definition (for each input pulse)

Table 43 DRAM CMD/ADR, CS Parameter Table

Symbol	Parameter	DQ-1333/1600/1867	DQ-3200	DQ-4266	Unit	Remar

		Min	Max	Min	Max	Min	Max		ks
VcIVW	Rx Mask Voltage - pk-pk	-	175	-	155	-	145	mV	1,2,3
TcIVW	Rx Input Valid Window	-	0.3	-	0.3	-	0.3	UI	
VIHL_AC	CA AC Input Pulse Amplitude pk-pk	210	-	190	-	180	-	mV	4,7
TcIPW	CA Input Pulse Width	0.55		0.6		0.6		UI	5
SRIN_cIVW	Input Slew Rate Above VcIVW	1	7	1	7	1	7	V/ns	6

a. The following Rx voltage and absolute timing requirements apply to all speed grades with DQ operating frequency of 1333 MT/s or lower. For example, at operating frequency of 1333 MT/s or lower, TcIVW = 450 ps.

Note:

1. CA Rx Mask Voltage and Pin Timing Parameters, including voltage and temperature drift.
2. The total Rx mask voltage VcIVW (maximum) must be centered around Vcent_CA (pin midpoint).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. The CA input receiver pulse signal amplitude must meet or exceed VIHLAC at any point in the total UI. There is no timing requirement above this level. VIHLAC is the peak-to-peak voltage centered at Vcent_CA (pin midpoint). The minimum VIHL_AC/2min must be satisfied both above and below Vcent_CA.
5. CA minimum input pulse width is defined only at Vcent_CA (pin midpoint).
6. Input slew rates that exceed the VcIVW mask, centered at Vcent_CA (pin midpoint).
7. VIHL_AC does not need to be satisfied when no transitions occur.

10.5 DRAM Data Timing

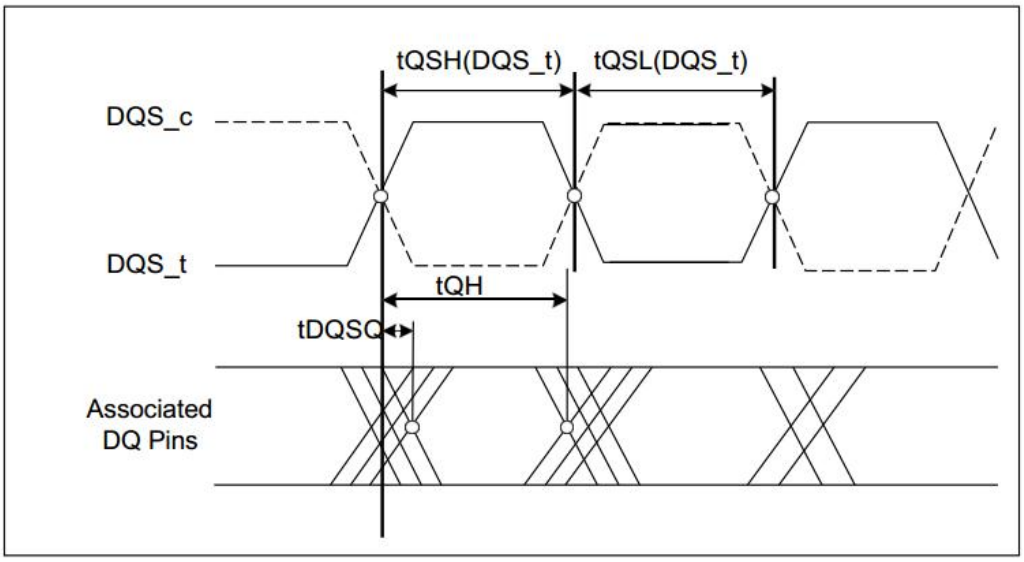


Figure 29 Read Data Timing Definition Diagram for tQH and tDQSQ for All DQ Signals in Each DQS Group

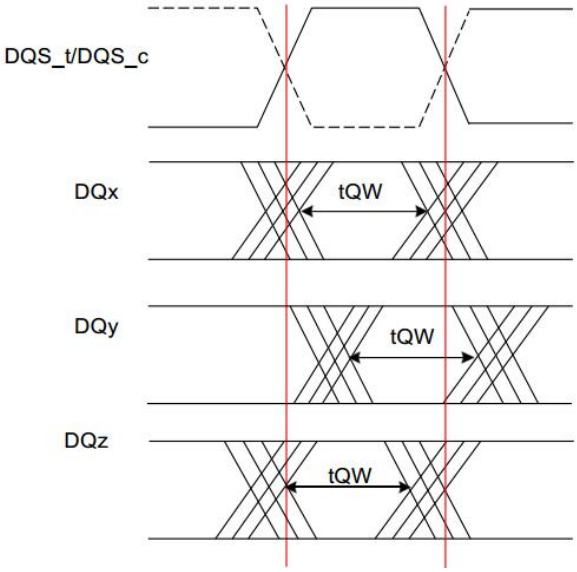


Figure 30 Read Data Timing tQW Valid Window Defined for Each DQ Signal

Table 44 Read Output Timing

Symbol	Parameter	DQ-1600/1866		DQ-2133/2400		DQ-3200		DQ-4266		Unit	Remarks
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
tDQSQ	DQS_t, DQS_c to DQ skew total, per group, per access (DBI disabled)	-	0.18	-	0.18	-	0.18	-	0.18	UI	
tQH	DQ output hold time from DQS_t, DQS_c (DBI disabled)	Min (tQSH, tQSL)	-	Min (tQSH, tQSL)	-	Min (tQSH, tQSL)	-	Min (tQSH, tQSL)	-	UI	
tQW_total	Total DQ output window time per pin (DBI disabled)	0.75	-	0.73	-	0.7	-	0.7	-	UI	3
tQW_dj	Deterministic DQ output window time per pin (DBI disabled)	TBD	-	TBD	-	TBD	-	TBD	-	UI	2,3
tDQSQ_DBI	DQS_t, DQS_c to DQ skew total, per group, per access (DBI enabled)	-	0.18	-	0.18	-	0.18	-	0.18	UI	6
tQH_DBI	DQS_t, DQS_c to DQ output hold time (DBI enabled)	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	TBD	UI	
tQW_total_DBI	Per-pin DQ output window time (DBI enabled)	0.75	-	0.73	-	0.7	-	0.7	-	UI	3
Data Strobe Timing											
tQSL	DQS, DQS# differential output low time (DBI disabled)	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK (avg)	3,4

tQSH	DQS, DQS# differential output high time (DBI disabled)	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK (avg)	3,5
tQSL _DBI	DQS, DQS# differential output low time (DBI enabled)	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK (avg)	4,6
tQSH _DBI	DQS, DQS# Differential Output High Time (DBI Enabled)	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK (avg)	5,6

a. The following receiver (Rx) voltage and absolute timing requirements apply to all speed bins with DQ operating frequency 1333 or lower. For example, at operating frequency 1333 or lower, tCIVW = 450 ps.

Note:

1 Deterministic portion of total timing. Measurement method TBD.

2 This parameter is determined and guaranteed by design.

3 This parameter is a function of input clock jitter. These values assume minimum tCH(abs) and tCL(abs). When input clock jitter minimum tCH(abs) and tCL(abs) are 0.44 of tCK(avg) or greater, the minimum of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs)-0.04.

4 tQSL describes the differential output low pulse width on DQS_t - DQS_c, from the falling edge to the next rising edge.

5 tQSH describes the differential output high pulse width on DQS_t - DQS_c, from the rising edge to the next falling edge.

6 This parameter is a function of input clock jitter. These values assume minimum values of tCH(abs) and tCL(abs). When the input clock jitter minimum tCH(abs) and tCL(abs) are 0.44 of tCK(avg) or greater, the minimum value of tQSL will be tCL(abs) - 0.04, and tQSH will be tCH(abs) - 0.04.

10.6 DQRx Voltage and Timing

DQ receive level and timing masks apply to each pin. The total mask (VdIVW_total, TdiVW_total) defines the region where the input signal must not intrude to allow the DQ receiver to successfully capture the input signal with a bit error rate (BER) less than tbd.

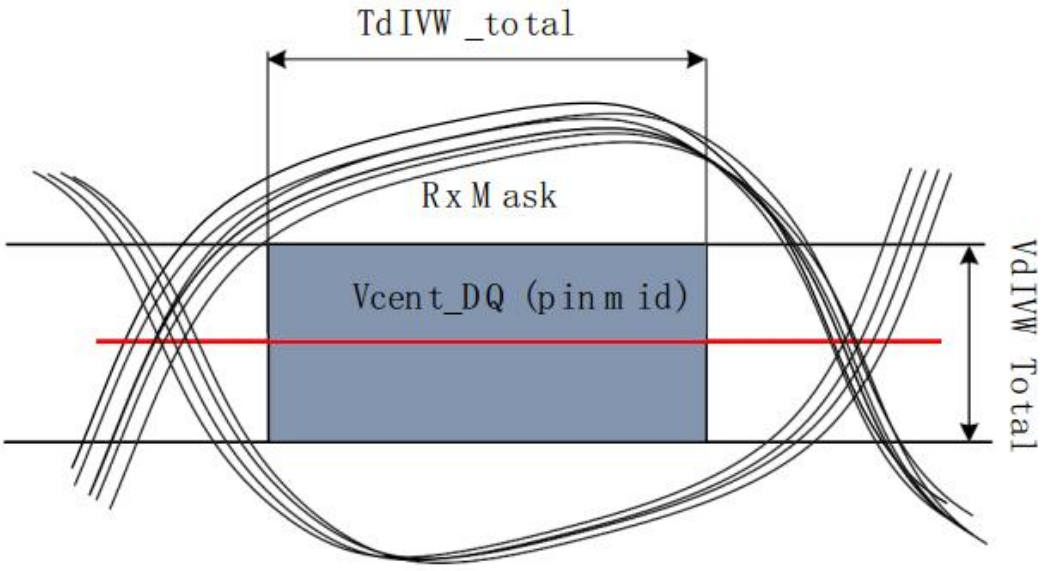


Figure 31 DQ Receiver Mask Diagram

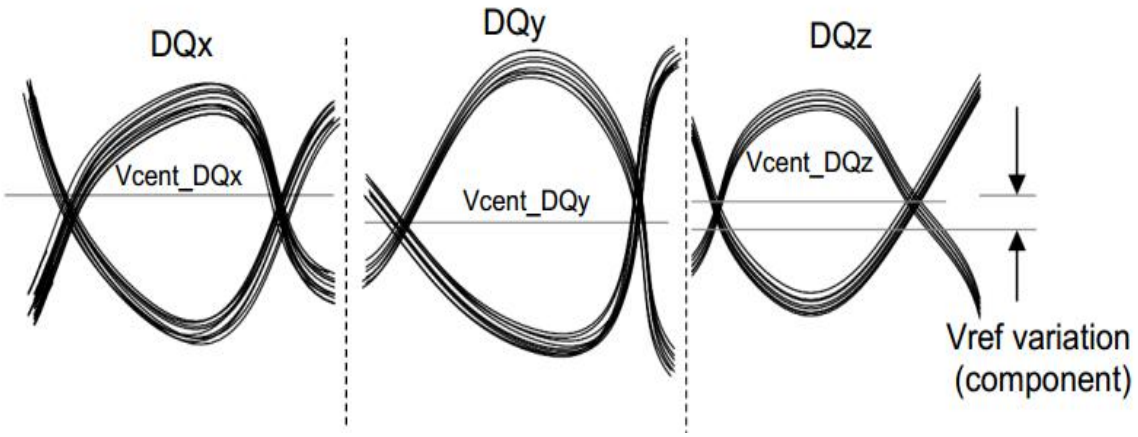


Figure 32 Cross-Pin VrefDQ Voltage Variation

Vcent_DQ(pin_mid) is defined as the midpoint between the maximum and minimum Vcent_DQ voltage levels across all DQ pins of a given DRAM device. As shown in Figure 32, each Vcent_DQ is defined by the center (i.e., widest opening) of the cumulative data input eye. This implies that any DRAM device level variation must be accounted for in the DRAMRx mask. Vref will be set by the system for Ron and ODT settings.

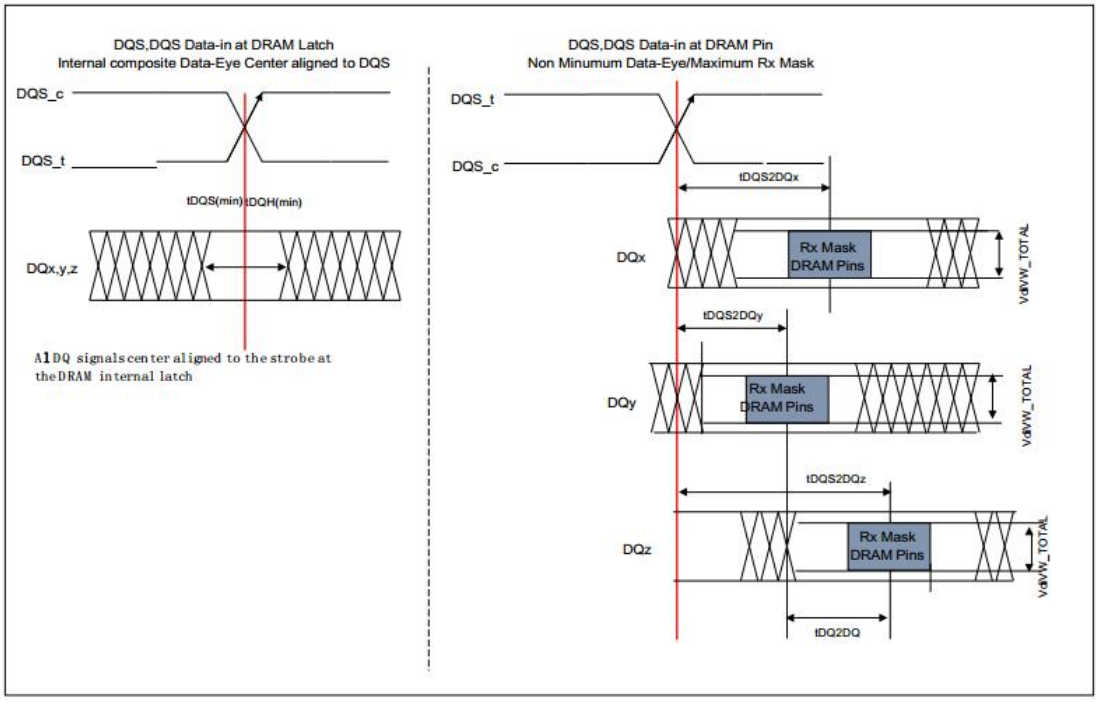


Figure 33 tDQS2DQ and tDQ2DQS Timing from DRAM Pin to DQS Referenced to Internal Latch

Note:

1. tDQS2DQ is measured at the center (midpoint) of the tDIVW window;
2. In this example, DQz represents the maximum tDQS2DQ;
3. DQy represents the minimum tDQS2DQ in this example;

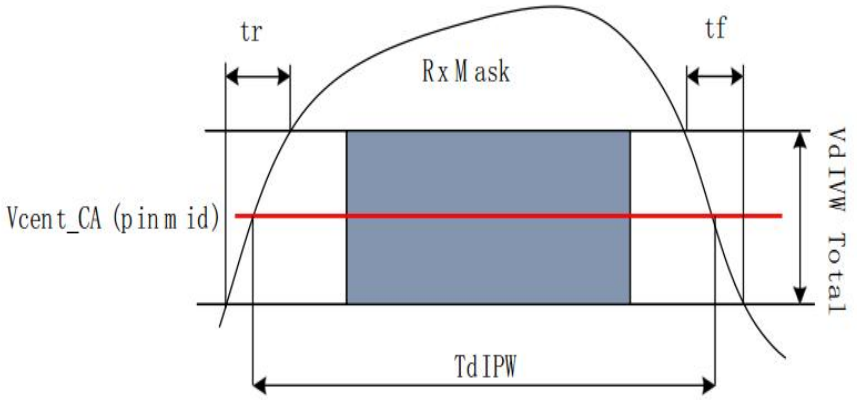


Figure 34 tDIPW and SRIN_dIVW Definition (for each input pulse)

Note: SRIN_dIVW = VdIVW_Total / (tr or tf). The signal must be monotonic within the tr and tf range.

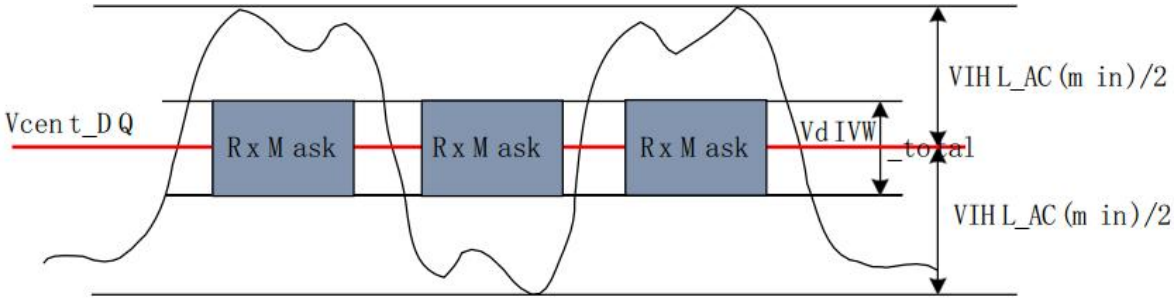


Figure 35 DQ VIH_AC/VIL_AC Definition

Table 45 DRAM DQ Receive Mode Parameters

*UI = tCK(avg) / 2

Symbol	Parameter	DQ-1600/1866/2133/2400		DQ-3200		DQ-4266		Unit	Remarks
		Min	Max	Min	Max	Min	Max		
VdIVW_total	Rx Mask Voltage - p-p Total	-	140	-	140	-	120	mV	1,2,3,4
TdIVW_total	Receiver Timing Window Total (at VdIVW Voltage Level)	-	0.22	-	0.25	-	0.25	UI	1,2,4
TdIVW_1bit	Receiver Timing Window 1-Bit Switching (at VdIVW Voltage Level)	-	TBD	-	TBD	-	TBD	UI	1,2,4,12
VIHL_AC	DQ AC Input Pulse Amplitude pk-pk	180	-	180	-	170	-	UI	5,13
TdIPWDQ	Input Pulse Width (at Vcent_DQ)	0.45		0.45		0.45	-	UI	6
tDQS2DQ	DQS to DQ Skew	200	800	200	800	200	800	ps	7
tDQ2DQ	DQ to DQ Skew	-	30	-	30	-	30	ps	8
tQSL	DQ to DQS Skew Temperature Variation	-	0.6	-	0.6	-	0.6	ps/℃	9

tDQS2DQ_volt	DQ to DQS Voltage Offset	-	33	-	33	-	33	ps/50 mV	10
SRIN_dIVW	Input Slew Rate above VdIVW_total	1	7	1	7	1	7	V/ns	11
tDQS2DQ_rank2rank	Inter-rank offset between DQ and DQS	-	200	-	200	-	200	ps	14,15,16

a. Rx voltage and absolute timing requirements apply to all speed grades with DQ operating frequency at or below 1600. For example, when the operating frequency is 1600 or lower, TdIVW_total(ps) = 137.5ps.

Note:

1. Data Rx mask voltage and timing parameters apply to each pin, including the effects of DRAM DQ to DQS voltage AC noise at frequencies > 20 MHz, and the maximum voltage of 45 mV pk-pk from DC to 20 MHz at fixed temperature on the package. The power supply voltage noise must meet the component minimum and maximum DC operating conditions.
2. The design specification is BER < TBD. When necessary, the BER will be characterized and extrapolated using the Dual-Dirac method.
3. The Rx mask voltage VdIVWtotal(max) must be centered at Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. The DQ input pulse amplitude entering the receiver must meet or exceed VIH_AC at any point across the entire UI. No timing requirements exist above the VIH_AC level. VIH_AC and VIL_AC are peak-to-peak voltages centered at Vcent_DQ(mid); VIH_AC(min) and VIL_AC(min) must simultaneously meet the requirements above and below Vcent_DQ.
6. The minimum input pulse width for DQ only is defined by Vcent_DQ(pin_mid).
7. DQ-to-DQS skew refers to the intra-byte skew from the DRAM pin to the internal latch. It includes all DRAM process, voltage, and temperature variations.
8. DQ-to-DQ skew from the DRAM pin to the internal latch, defined within the same byte.
9. tDQS2DQ maximum delay variation as a function of temperature.
10. tDQS2DQ maximum delay variation as a function of VDDQ and VDD2 DC voltage variation. It includes VDDQ and VDD2 AC noise effects at frequencies > 20 MHz, and a maximum voltage of 45 mV pk-pk from DC to 20 MHz at a fixed temperature on the package. The test assumes VDDQ = VDD2.
11. Input slew rate centered on Vcent_DQ(pin_mid), exceeding the VdIVW mask.
12. Receiver mask definition: one pin switching simultaneously with other DQ signals in a steady state.
13. When no transition occurs, VIHL_AC does not need to meet the requirement.
14. Same voltage and temperature apply to tDQS2DQ_rank2rank.
15. The tDQS2DQ_rank2rank parameter applies to multiple ranks per byte lane within a package composed of identically designed chips.
16. The tDQS2DQ_rank2rank parameter has been added to JESD209-4B. Some legacy devices supporting JESD209-4 and JESD209-4A may not support this parameter. Refer to the supplier datasheet.

11. AC Timing Parameters

11.1 Core Timing

Table 46 Core Timing Parameters

Parameter	Symbol	Min/Max	Data Rate	Unit
Core Timing Parameters			533/1066/1600/2133/2667/3200/3733/4267	
Activate to Activate Command Period (Same Bank Group)	tRC	MIN	tRAS + tRPab (All Bank Precharge) tRAS + tRPpb (Per Bank Group Precharge)	ns
Frequency Set Point Switching Time (Middle)	tSR	MIN	max(15ns, 3nCK)	ns

(Entry to Exit)				
Self-refresh exit to next valid command delay	tXSR	MIN	max(tRFCab + 7.5ns, 2nCK)	ns
Power-down exit to next valid command delay	tXP	MIN	max(7.5ns, 5nCK)	ns
CAS-to-CAS delay	tCCD	MIN	8	tCK (avg)
Internal read to precharge command delay	tRTP	MIN	min(7.5ns, 8nCK)	ns
RAS to CAS Delay	tRCD	MIN	Min (18 ns, 4 nCK)	ns
Row Precharge Time (Single Bank)	tRPpb	MIN	Max (18 ns, 4 nCK)	ns
Row Precharge Time (All Banks)	tRPab	MIN	Min (21 ns, 4 nCK)	ns
Row Active Time	tRAS	Max	MIN (42 ns, 3 nCK)	ns
Row Active Time	tRAS	MIN	MIN (9 × tREFI, 70.2) µs	µs
Write Recovery Time	tWR	MIN	MIN (18 ns, 6 nCK)	ns
Write-to-Read Delay	tWTR	MIN	MIN (10 ns, 8 nCK)	ns
Activate Bank A to Activate Bank B	tRRD	MIN	MIN (10 ns, 4 nCK)	ns
Precharge to Precharge Delay	tPPD	MIN	4	tCK
Four-Bank Activation Window	tFAW	MIN	40	ns
Note:				
The precharge-to-precharge timing constraint does not apply to auto precharge commands.				

11.2 Core Read Timing

Table 47 Core Read Timing Parameters

Parameter	Symbol	Min/Max	Data Rate	Unit
Core Parameter			533/1066/1600/2133/2667/3200/3733/4267	
Read Preamble Time	tRPRE	MIN	1.8	tCK (avg)
0.5 tCK Read Postamble	tRPST	MIN	0.4	tCK (avg)
1.5tCK Read Preamble	tRPST	MIN	1.4	tCK (avg)
DQ Low Impedance Response Time	tLZ(DQ)	MIN	(RL×tCK) + tDQSCK(Min) - 200ps	ps
DQ Low Impedance Response Time	tHZ(DQ)	Max	(RL×tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2×tCK) - 100ps	ps
DQS Low Impedance	tLZ(DQS)	MIN	(RLxtCK) + tDQSCK(Min) - (tRPRE(Max) xtCK) + 200ps	ps

Response Time				
DQS High Impedance Response Time	tHZ(DQS)	Max	(RL × tCK) + tDQSCK(Max) + (BL/2 × tCK) + (RPST(Max) × tCK) - 100ps	ps
DQS-DQ Skew	tDQSQ	Max	0.18	UI

11.3 tDQSCK Timing

Table 48 Timing Table

Parameter	Symbol	Min	Max	Unit	Remarks
Output response time from CK_t/CK_c to DQS	tDQSCK	1.5	3.5	ns	1
Temperature variation during output response from CK_t/CK_c to DQS	tDQSCK_temp	-	4	ps/℃	2
Voltage variation during output response from CK_t/CK_c to DQS	tDQSCK_volt	-	7	ps/mV	3
Note:					
1. Includes DRAM process, voltage, and temperature variations. It includes the effects of AC noise at frequencies greater than 20 MHz, and a maximum voltage of 45 mV pk-pk from DC to 20 MHz at a fixed temperature on the package. Supply voltage noise must comply with the device minimum and maximum DC operating conditions.					
2. tDQSCK_temp Maximum delay variation as a function of temperature.					
3. tDQSCK_volt Maximum delay variation as a function of VDDQ and VDD2 DC voltage changes. tDQSCK_volt is used to calculate timing variations caused by VDDQ and VDD2 noise below 20 MHz. The host controller does not need to consider any variations due to VDDQ and VDD2 noise above 20 MHz. Power supply voltage noise must meet the device minimum and maximum DC operating conditions. Voltage variation is defined as Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. Tester measurement assumes VDDQ = VDD2.					

Table 49 CK to DQS Rank Delay Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Remarks
DQS Output Clock Delay Time			1600/1866/2133/2667/3200/4267		
CK to DQS Rank-to-Rank Delay	tDQSCK_rank to rank	Max	1	ns	1,2
Note:					
1. Use the same voltage and temperature for tDQS2CK_rank2rank.					
2. The tDQSCK_rank2rank parameter applies to multi-rank per byte channel in packages consisting of chips of the same design.					

11.4 AC Write Timing

Table 50: Write Timing Parameters

Parameter	Symbol	Min/Max	Data Rate	Unit
Write Pulse Width			533/1066/1600/2133/ 2667/3200/3733/4267	
Write Command to First DQS Latching Edge	tDQSS	Min	0.75	tCK (avg)
		Max	1.25	
DQS input high pulse width	tDQSH	Min	0.4	tCK (avg)
DQS input low pulse width	tDQSL	Min	0.4	tCK (avg)
DQS Falling Edge to CK Setup Time	tDSS	Min	0.2	tCK (avg)
CK to DQS Falling Edge Hold Time	tDSH	Min	0.2	tCK (avg)
Write Postamble Time	tWPRE	Min	1.8	tCK (avg)
0.5 tCK Write Postamble Time	tWPST1	Min	0.4	tCK (avg)
1.5 tCK Write Postamble Time	tWPST1	Min	1.4	tCK (avg)
Note: The duration of write leveling depends on the setting of MR3 OP1.				

11.5 Self-Refresh Time

Table 51 Self-Refresh AC Timing Parameters

Parameter	Symbol	Min/Max	Data Rate	Unit	Remarks
			533/1066/1600/2133/2667/3200/3733		
Self-Refresh Timing Parameters					
Delay from SRE Command to CKE Input Low	tESCKE	Min	Min (1.75 ns, 3 tCK)	ns	1
Minimum Self-Refresh Time	tSR	Min	Min (15 ns, 3 tCK)	ns	1
Exit Self-Refresh to Active Command	tXSR	Min	Minimum (tRFCab + 7.5 ns, 2 tCK)	ns	2
Note:					
The delay must satisfy both the analog time (ns) and the clock cycle count (tCK) requirements. This means that tESCKE is satisfied only after CK has switched for at least 3 full cycles (3 × tCK) and 1.75 ns.					

11.6 Mode Register Read/Write AC Timing

Table 52 Register Read/Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Mode Register Read/Write Timing				

Additional time after tXP until MRR command can be issued	tMRRI	Min	tRCD + 3nCK	-
Mode Register Read Command Cycle	tMRR	Min	8	nCK
Mode Register Write Command Cycle	tMRW	Min	MAX(10ns,10nCK)	-
Mode register set command delay	tMRD	Min	MAX(14 ns, 10 nCK)	-

11.7 VRCG Enable/Disable Timing

Table 40 Enable/Disable Timing Table

Data Rate		533/1066/1600/2133/ 2667/3200/3733/4267		Unit
Parameter	Symbol	Min	Max	
VREF High Current Mode Enable Time	tVRCG_ENABLE	-	200	ns
VREF High Current Mode Disable Time	tVRCG_DISABLE	-	100	ns

11.8 Bus Command Training Timing

Table 41 Bus Command Training Timing

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/ 2667/3200/3733/4267	
Bus Command Training Timing	tCKELCK	Min	Max (5ns, 5nCK)	-
Data Setup Pattern for VREF Training	tDStrain	Min	2	ns
Data Hold for VREF Training	tDHtrain	Min	2	ns
Asynchronous Data Read	tADR	Max	20	ns
CA bus training command delay	tCACD2	Min	RU(tADR/tCK)	tCK
Time from CKE low to valid strobe	tDQSCKE1	Min	10	ns
First CA bus training time after CKE low	tCAENT	Min	250	ns
VREF step time - multiple steps	tVREFCA_LONG	Max	250	ns
VREF Step Time – Single Step	tVREFCA_SHORT	Max	80	ns
Valid Clock Requirement Before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))	-
Valid Clock Requirement After CS High	tCKPSTCS	Min	max(7.5ns, 5nCK)	-

Minimum Delay from CS to DQS	tCS_VREF	Min	2	tCK
Minimum delay from CKE high to DQS high impedance	tCKEHDQS	Min	10	ns
Minimum valid clock requirement before CKE high	tCKCKEH	Min	Max (1.75 ns, 3 nCK)	-
After exiting CA training, setting CKE high places DQ into high impedance	tMRZ	Min	1.5	ns
ODT turn-on delay from CKE	tCKELODTon	Min	20	ns
ODT turn-off delay from CKE	tCKELODToff	Min	20	ns
Exit command bus training mode to next valid command delay	tXCBT_Short	Min	Maximum (5nCK, 200ns)	-
	tXCBT_Middle	Min	Maximum (5nCK, 200ns)	-
	tXCBT_Long	Min	Maximum (5nCK, 250ns)	-
Note:				
1. During tDQSCKE, DQS_t must be low and DQS_c must be high.				
2. If tCACD is violated, the sampled data violating tCACD will not be available, except for the last sample (after which tCACD is compliant). Valid data for the last sample will be provided after tADR.				
3. The delay time from exiting command bus training mode to the next valid command depends on the VREF(CA) setting: MR12 OP[5:0] and VREF(CA) range; see Table 61 for details. Additionally, the delay time from exiting command bus training mode to the next valid command may affect the VREF(DQ) setting. The settling time for VREF(DQ) level is the same as for VREF(CA) level.				

Table 42 Command Bus Training Timing for Mode 1

Parameter	Symbol	Min/Max	Data Rate	Unit	Remarks
			533/1066/1600/2133 2667/3200/3733/4267		
Command Bus Training Timing					
Clock and Command Valid (after CKE Low)	tCKELCK	Min	Maximum (7.5 ns, 3 nCK)	tCK	
Asynchronous Data Read	tADR	Max	20	ns	
Minimum CA Bus Training Command to Command Delay (tCACD)	tCACD	Min	RU(tADR/tCK)	tCK	1
First CA Bus Training Command after CKE Goes Low	tCAENT	Min	250	ns	
Valid Clock Requirement Before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))		
Active clock requirement After CS high	tCKPSTCS	Min	max(7.5ns, 5nCK))		
Clock and command valid before CKE high	tCKCKEH	Min	2	tCK	
Control address bus training: set CKE high to tristate DQ bus	tMRZ	Min	1.5	ns	

ODT turn-on delay from CKE	tCKELODTon	Min	20	ns	
ODT turn-off delay from CKE	tCKELODToff	Min	20	ns	
Delay from exiting command bus training mode to entering next valid command	tXCBT_Short	Min	Maximum (5nCK, 200ns)		2
	tXCBT_Middle	Min	Maximum (5nCK, 200ns)		2
	tXCBT_Long	Min	Maximum (5nCK, 250ns)		2
Note:					
If tCACD is violated, no valid sampled data can be obtained, except for the last sample (the tCACD after that sample meets the requirement). Valid data for the last sample will be provided after tADR.					
2. The delay from exiting command bus training mode to the next valid command depends on the VREF(CA) setting: MR12 OP[5:0] and VREF(CA) range. Additionally, the delay from exiting command bus training mode to the next valid command may affect the VREF(DQ) setting. The settling time of the VREF(DQ) level is the same as the VREF(CA) level.					

Table 43 Command Bus Training Timing for Mode 2

Parameter	Symbol	Min/Max	Data Rate	Unit	Remarks
			533/1066/1600/2133 2667/3200/3733/4267		
Active clock requirement after CKE LOW	tCKELCK	Min	Max (5ns, 5nCK)	ns	
Valid Clock Requirement Before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))	-	
Valid Clock Requirement After CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))	-	
Valid Strobe Requirement Before CKE Low	tDQSCKE	Min	10	ns	1
First CA Training Command After CKE Low	tCAENT	Min	250	ns	
VREF Step Time - Long	tVREFCA_Long	Max	250	ns	2
VREF Step Time - Middle	tVREFCA_Middle	Max	200	ns	3
VREF Step Time - Short	tVREFCA_Short	Max	100	ns	4
VREF Training Data Setup Time	tDStrain	Min	2	ns	
Vref Training Data Hold Time	tDHtrain	Min	2	ns	
Asynchronous Data Read Valid Window	tADVW	Min	16	ns	
		Max	80	ns	
DQS Input Cycle Time in CBT Mode	tDQSICYC	Min	5	ns	
		Max	100	ns	
Asynchronous Data Read	tADR	Max	20	ns	
DQS_c High from CS High Start	tHZCBT	Min	0	ns	

Time					
Asynchronous Data to DQ7 Setup Time	tAD2DQ7	Min	3	ns	
		Max	10	ns	
DQ7 Hold Time	tDQ7SH	Min	10	ns	
		Max	60	ns	
Asynchronous Data Read Pulse Width	tADSPW	Min	3	ns	
		Max	10	ns	
Hi-Z to Async Vref- CA Valid Data	tHZ2VREF	Min	Maximum (10 ns, 5 nCK)	-	
CBT Read-to-Write Delay	tCBTRTW	Min	2	ns	
Delay Between Two CA Training Commands	tCACD	Min	110 ns (or 4 nCK)		
Minimum Time Delay from Clock Enable (CKE) High to DQS High-Impedance	tCKEHDQS	Min	10	ns	
Clock and Command Valid Before CKE High	tCKCKEH	Min	Max (1.75 ns, 3 nCK)		
ODT Enable Delay from CKE	tCKELODTon	Max	20	ns	
ODT Disable Delay from CKE (ODT_CA)	tCKELODToff	Max	20	ns	
ODT Disable from CKE for ODT_DQ and DQS	tCKEH_ODT_off	Max	20	ns	
Delay from CS high to ODT_DQ turn-off during CB training	tODToff_CBT	Max	20	ns	
Delay from end of valid data output to ODT_DQ turn-on	tODTon_CBT	Max	Maximum (10 ns, 5 nCK)		
Delay from exiting command bus training mode to entering next valid command	tXCBT_Short	Min	Maximum (5nCK, 200ns)		5
	tXCBT_Middle	Min	Maximum (5nCK, 200ns)		5
	tXCBT_Long	Min	Maximum (5nCK, 250ns)		5
Note:					
1. During tDQSCKE, DQS_t must be low and DQS_c must be high.					
2. VREFCA_long is the transition time of the VREF voltage from VREFmin to VREFmax or from VREFmax to VREFmin within the VREFDQ range.					
3. VREF_Middle refers to a change of at least two levels (increment or decrement) of the VREF voltage within the same VREFDQ range. VREF_Short is used for a single-level change of the VREF voltage.					
5. The delay from exiting command bus training mode to the next valid command depends on the VREF(CA) setting: MR12OP[5:0] and the VREF(CA) range: MR12OP[6] for FSP-OP0 and 1.					

11.9 Frequency Set Point Timing

Table 57 Frequency Set Point Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133 2667/3200/3733/4267	

Frequency Set Point Parameters				
Frequency Set Point Switching Time	tFC_Short1	Min	200	ns
Frequency Set Point Switching Time (Middle)	tFC_Middle1	Min	200	ns
Frequency Set Point Switching Time (Long)	tFC_Long1	Min	250	ns
Valid Clock Input Requirement after FSP Change	tCKFSPE	Min	Max (7.5 ns, 4 nCK)	-
Valid clock requirement after FSP change before first valid command	tCKFSPX	Min	Max (7.5ns, 4nCK)	-
Note:				
Frequency set point switching time depends on VREF(CA) setting: MR12OP[5:0] and VREF(CA) range for FSP-OP0 and FSP-OP1. In addition, frequency set point change may affect VREF(DQ) setting. VREF(DQ) level settling time is the same as VREF(CA) level.				

11.10 Write Leveling Timing

Table 58 Write Leveling Timing Table

Parameter	Symbol	Min/Max	Reference Value	Unit
DQS_t/DQS_c Delay after Write Leveling Programming	tWLDQSEN	Min	20	tCK
		Max	-	
Write Leveling after Write Synchronization	tWLWPRE	Min	20	tCK
		Max	-	
First DQS_t/DQS_c Edge after Write Leveling Mode Programming	tWLMRD	Min	40	tCK
		Max	-	
Write Leveling Output Delay	tWLO	Min	0	ns
		Max	20	
Mode register set command delay	tMRD	Min	Max (14 ns, 10 tCK)	ns
		Max	-	
Valid clock requirement before DQS triggering	tCKPRDQS	Min	Max (7.5ns, 4nCK)	-
		Max	-	
Valid Clock Requirement after DQS Toggle	tCKPST_DQS	Min	Max (7.5ns, 4nCK)	-
		Max	-	

Table 59 Write Leveling Setup and Hold Timing Table

Parameter	Symbol	Min/Max	Data Rate				Unit
			1600	2400	3200	4266	
Write Leveling Parameters							
Write Leveling Hold Time	tWLH	Min	150	100	75	50	ps
Write Leveling Setup Time	tWLS	Min	150	100	75	50	ps
Write Leveling Input Valid Window	tWLIVW	Min	240	160	120	90	ps

11.11 MPC Write FIFO Timing

Table 60 Write FIFO Timing Diagram

Parameter	Symbol	Min/Max	Data Rate
			533/1066/1600/2133/2667/3200/3733
MPC Write FIFO Timing			
Additional time after tXP before MPC [Write FIFO] command can be issued	tMPCWR	Min	tRCD + 3nCK

11.12 DQS Internal Oscillator Timing

Table 61 DQS Internal Oscillator Timing

Parameter	Symbol	Min/Max	Reference Value	Unit
Oscillator period to mode register read delay time	tOSCO	Min	Max (40 ns, 8 nCK)	ns
Note:				
The DQS oscillator command must not be issued before tOSCO (minimum) is satisfied.				

11.13 Read Postamble Training Timing

Table 62 Read Postamble Training Timing

Parameter	Symbol	Min	Max
Delay from MRW Command to DQS Drive	tSDO	-	Max (12 nCK, 20 ns)

11.14 ZQ Calibration Timing

Table 63 ZQ Calibration Timing Table

Parameter	Symbol	Min/Max	Reference Value	Unit
ZQ Calibration Time	tZQCAL	Min	1	us
ZQ Calibration Lockout Time	tZQLAT	Min	Max (30 ns, 8 nCK)	ns
ZQ Calibration Reset Time	tZQRESET	Min	max(50ns,3nCK)	ns

11.15 ODTCA AC Timing

Table 64 ODTCA AC Timing Table

Speed		1600/1866/2133/2400/3200/4266	
Parameter	Symbol	MIN	Max
ODTCA Value Update Time	tODTUP	RU (TBD ns/tCK (average))	-

11.16 Power-Down Sequence

Table 65 Power-Down Sequence

Parameter	Symbol	Min/Max	Data Rate	Unit	Remarks
			533/1066/1600/2133 2667/3200/3733		
CKE minimum pulse width (high and low level pulse width) tCKE	tCKE	Min	Maximum (7.5 ns, 4 nCK)	-	
Delay from valid command to CKE	tCMDCKE	Min	Max (1.75 ns, 3 nCK)	ns	1

input low					
Valid clock requirement after CKE input low	tCKELCK	Min	Max (5ns, 5nCK)	ns	1
CS valid requirement before CKE input low	tCSCKE	Min	1.75	ns	
CS Hold Time After CKE Low	tCKELCS	Min	Max (5ns, 5nCK)	ns	
Clock Setup Time Before CKE High	tCKCKEH	Min	Max (1.75 ns, 3 nCK)	ns	1
Delay from Power-Down Exit to Next Valid Command	tXP	Min	Min (7.5 ns, 5 nCK)	ns	1
Setup time of CS valid before CKE high	tCSCKEH	Min	1.75	ns	
Hold time of CS valid after CKE high	tCKEHCS	Min	Max (7.5 ns, 5 nCK)	ns	
Valid clock and CS requirement after MRW command before CKE goes low	tMRWCKEL	Min	Max (14 ns, 10 nCK)	ns	1
ZQ calibration start command to CKE low valid clock and CS requirement	tZQCKE	Min	Max (1.75 ns, 3 nCK)	ns	1
Note: The delay time must satisfy both the analog time (ns) and clock cycle count (nCK) requirements.					