

Loongtion®

DDR5 SDRAM
Datasheet

Ningbo Ningbo Loongtion Intelligent Technology Co., Ltd.
Email: hi@loongtion.com Tel: +86-400-851-6832, +86-138-0587-8152 Web: www.loongtion.com

Revision History

Version	Update Date	Description
Rev 1.0	2025/09	Initial Draft
Rev 1.1	2025/10	Changed package outline drawing

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1. Product Introduction

This product uses DDR5 wafers from Hefei ChangXin (CXMT) and has been packaged and temperature screened according to the characteristics of industrial and specific embedded applications, offering excellent stability and performance characteristics.

1.1 Speed Parameter

Table 1-1 Speed Parameters

Speed CL-nRCD-nRP	DDR5-4800	DDR5-5600	DDR5-6400	Unit
	40-39-39	46-45-45	52-52-52	
tCK (min)	0.416	0.357	0.313	ns
CAS Latency	40	46	52	nCK
tRCD	16	16	16	ns
tRP	16	16	16	ns
tRAS	32	32	32	ns
tRC	48	48	48	ns

1.2 Key Features

- Compliant with JEDEC standards;
- Power Supply: VDD/VDDQ = 1.1V (1.067V (-3%) to 1.166V (+6%));
- Power Supply: VPP = 1.8V ±5% (1.71V to 1.89V);
- JEDEC Standard Packages: x4/x8 in 82-ball WBGA, x16 in 102-ball WBGA;
- Array Configuration:
- x4/x8 Configuration: 32 Banks (8 Bank Groups, 4 Banks per Bank Group);
- **16 Banks (4 Bank Groups, 4 Banks per Bank Group) for x16;**
- 16n-Bit Prefetch Architecture;
- Burst Length (BL) Support: BL16, BC8 OTF, BL32 (Optional), BL32 OTF (Optional);
- Programmable CAS Latency (CL);
- Programmable CAS Write Latency (CWL);
- On-Die Termination (ODT) through mode register settings: RTT_PARK, RTT_NOM, RTT_WR; RTT_NOM_RD, DQS_RTT_PARK
- Same-bank and all-bank refresh in normal refresh mode and fine-granularity refresh mode;
- Fine-granularity refresh mode: 2x (0°C ≤ TCase ≤ 85°C), 4x (85°C < TCase ≤ 95°C) for reduced tRFC;

- Bidirectional differential data strobe signals (DQS_t/DQS_c);
- POD (Pseudo Open Drain) interface for data input/output, command, and address input;
- Supports connectivity test mode (TEN);
- Internal VREF for data input, command and address input, and chip select;
- CAI (Command Address Inversion);
- Support for 1N/2N command mode;
- Support for 4-tap decision feedback equalizer (DFE);
- Support for loopback test and bit error rate test;
- Support for hPPR/sPPR; support for sPPR execute/abort/lock;
- Training mode:
- VrefDQ/VrefCA/VrefCS training
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per-Pin VREFDQ Training
- Write Leveling Training Mode
- Duty Cycle Adjuster (DCA) for Read - Global
- Read Dedicated Per-Pin DCA (Duty Cycle Adjuster) – Per-Pin (DQ)
- Per DRAM Addressability (PDA)
- Maximum Power Saving Mode (MPSM);
- Multi-Purpose Command (MPC);
- Asynchronous reset at power-up;
- Operating case temperature: 0°C ≤ TCASE ≤ 95°C;
- Supports auto-refresh and self-refresh modes;
- Average refresh interval:
- **3.9 µs / 32 ms, 8K cycles (0°C ≤ TCASE ≤ 85°C);**
- **1.95 µs / 16 ms, 8K cycles (85°C < TCASE ≤ 95°C);**
- Programmable read and write preamble and postamble;
- Read and write data integrity supported via Cyclic Redundancy Check (CRC);
- On-die ECC error correction;
- ECC transparency and error scrubbing;

- MBIST/mPPR;
- Downshift mode not supported;
- Package output driver test mode;
- Partial Array Self Refresh (PASR) not supported;
- RoHS compliant

Note: The functions and timing specifications described in this datasheet apply to DLL enabled mode (normal operation) unless otherwise noted.

1.3 Product List

Table 1-2 Package Information

Density	Configuration	Package	Part Number	Operating Temperature
16Gb	2Gb×8	WBGA-82	YC5GG16W-9CXDQ-M(0)	-25/85
16Gb	2Gb×8	WBGA-82	YZ5GG16W-9CXDQ-M(0)	-40/85

1.4 Address Table

Table 1-3 16Gb Address Table

Parameter	4Gb x 4	2Gb × 8	1Gb × 16
Number of Bank Groups	8	8	4
Banks Per Bank Group	4	4	4
Bank Group Address	BG0-BG2	BG0-BG2	BG0-BG1
Bank Address in Bank Group	BA0-BA1	BA0-BA1	BA0-BA1
Row Address	R0-R15	R0-R15	R0-R15
Column Address	C0-C10	C0-C9	C0-C9
Page Size	1KB	1KB	2KB

2. DDR5 SDRAM Package Specifications

DDR5 SDRAM x4/x8/x16 Configuration Package Dimensions and Pinouts are as follows:

- SDRAM x4/x8 Pinout, MO-210-AN Package – 82-ball BGA
- SDRAM x16 Pinout, MO-210-AN Package – 102-ball BGA

2.1 DDR5 SDRAM Package Dimensions

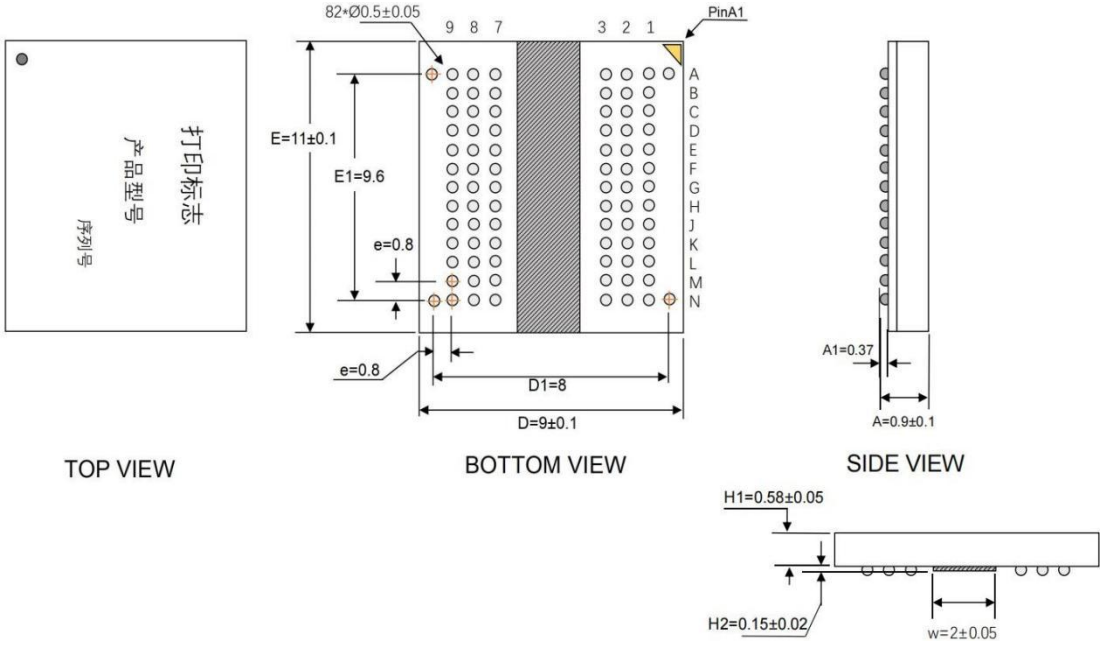


Figure 2-1 82-ball BGA – x4/x8 Component

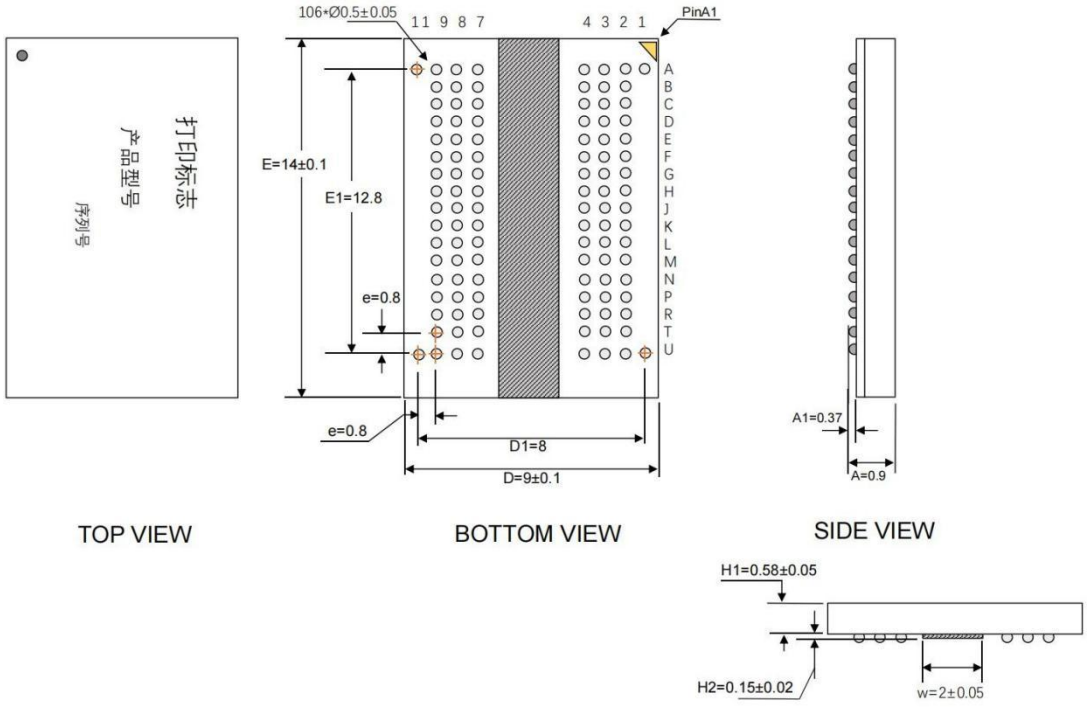


Figure 2-2 102-ball BGA – x16 Component

2.2 DDR5 SDRAM x4/x8 Ball Assignment

MO-210-AN – 82-ball package

AN / AL	1	2	3	4	5	6	7	8	9	10	11	AN / AL
		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ		D
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ		J
K		VDD	CA6	CA2				CA3	CA7	VDD		K
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ		L
M		CAI	CA10	CA12				CA13	CA11	RESET_n		M
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	N

注 1 DQ4-DQ7 是高阶 DQ 引脚，在 x4 配置中未连接。

注 2 TDQS_t 在 x4 配置中无效。

注 3 x4 配置下 TDQS_c 不可用 4 - x4 配置下 DM_n 无效。

Figure 2-3 DDR5 Ball Assignment for X4/X8 Component

Note:

1. MO-210 terminal pattern AN (x4/x8) pins with support balls are for mechanical support only and should not be connected to high or low logic levels.
2. DQ4-DQ7, the upper DQ pins, may be connected but not used in x4 configuration.
3. DM is not valid in x4 configuration.

2.3 DDR5 SDRAM x16 Ball Assignment

MO-210-AU – 102-ball

AU / AT	1	2	3	4	5	6	7	8	9	10	11	AU / AT
		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQU2				DQU3	VDDQ	VDD		B
C		VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS		C
D		VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ		D
E		VDD	DQU4	DQU6				DQU7	DQU5	VDD		E
F		VDD	VDDQ	DQL2				DQL3	VDDQ	VDD		F
G		VSS	DQL0	DQSL_t				DML_n	DQL1	VSS		G
H		VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ		H
J		VDD	DQL4	DQL6				DQL7	DQL5	VDD		J
K		VSS	VDDQ	VSS				VSS	VDDQ	VSS		K
L		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		L
M		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		M
N		VDDQ	CA4	CA0				CA1	CA5	VDDQ		N
P		VDD	CA6	CA2				CA3	CA7	VDD		P
R		VDDQ	VSS	CA8				CA9	VSS	VDDQ		R
T		CAI	CA10	CA12				CA13	CA11	RESET_n		T
U	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	U

Figure 2-4 DDR5 Pinout for X16 Component

Note: In the MO-210 terminal configuration AU (X16) with support balls, the additional inactive ball columns and rows are for mechanical support only and should not be connected to any electrical high or low level.

2.4 Pin Description

Table 2-1 Pin Description Table

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing point of the positive edge of CK_t and the negative edge of CK_c.
CS_n	Input	Chip Select: When CS_n is high, all commands are masked. CS_n is used for rank selection on multi-rank systems. CS_n is considered part of the command code. CS_n is also used for entering and exiting from power-down mode. Partial low-power mode.
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is the input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both rising and falling edges of the DQS signal. For x8 devices, this function is enabled via MR5:OP[5]=1. x4 devices do not support DM function. Function The device does not support the DM function.
CA [13:0]	Input	Command/Address Input: CA signals provide command and address inputs according to the command truth table. Note: Because some commands involve multi-cycle operations, pins are not interchangeable between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, inactive when HIGH. During normal operation, RESET_n must be HIGH. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW levels at 80% and 20% of VDDQ, respectively.
DQ	Input/Output	Data Input/Output: Bidirectional data bus. If CRC check is enabled via the mode register, the CRC code is appended at the end of the data burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/Output	Data Clock Pulse: Output when reading data, input when writing data. Edge-aligned, center-aligned for write data. For x16 bus, DQSL corresponds to DQL0-DQL7 data; DQSU corresponds to DQU0-DQU7 data. The data strobe signals DQS_t, DQSL_t, and DQSU_t are paired with the differential signals DQS_c, DQSL_c, and DQSU_c, respectively, providing differential pair signaling for the system during read and write operations. DDR5 SDRAM supports only differential data strobes and does not support single-ended mode.
TDQS_t, TDQS_c	Output	Termination data strobe signals: TDQS_t/TDQS_c are only applicable for x8 DRAM. When enabled by
Symbol	Type	Function

		MR5:OP[4]=1, the DRAM enables the same termination resistance function on TDQS_t/TDQS_c as on DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t provides the data mask function according to MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function by setting MR5:OP[4]=0. TDQS function is disabled by MR5:OP[4]=0.
ALERT_n	Input/Output	Alert: If a CRC error occurs, ALERT_n goes low for a period and then returns high. In connectivity test mode, this pin operates as an input. Whether to use this signal depends on the system. If not connected as a signal, the ALERT_n pin must be tied to VDDQ on the board.
TEN	Input	Connectivity test mode enable: Required for x4, x8, and x16 devices. When this pin is driven high, it enables connectivity test mode in conjunction with other pins. This is a CMOS rail-to-rail signal, with AC high and low levels at 80% and 20% of VDDQ, respectively. Whether to use this signal depends on the system. This pin may have an internal weak pull-down resistor to VSS. (Recommended to merge into previous paragraph; delete here.)
MIR	Input	Mirror: Used to inform the SDRAM device that the current configuration is in mirror mode rather than standard mode. When the MIR pin is connected (bridged) to VDDQ, the SDRAM internally swaps even CA with the adjacent higher odd CA. If CA mirror function is not needed, the MIR pin should typically be tied to VSS. Example mirror pairs: CA2 with CA3 (not CA1), CA4 with CA5 (not CA3). Note that the CA[13] function is only valid for certain densities. DRAM devices (including stacked configurations). If CA[13] is not used, its ball position (Regardless of whether the MIR function is enabled) should be connected to VDDQ. No valid signal drive requirements are defined.
CAI	Input	Command and Address Inversion: When the CAI pin is connected (paralleled) to VDDQ, the DRAM internally inverts the logic levels of all CA signals. If CA inversion is not required, the CAI pin should typically be connected to VSS. No valid signal requirements are defined.
CA_ODT	Input	Command and Address On-Die Termination (ODT) setting selection. If the pin is connected to VSS, the A group setting is applied; if the pin is connected to VDDQ, the B group setting is applied. This pin has no valid signal requirements.
LBDQ	Output	Loopback Data Output: Output of this device on the loopback output selection (defined by MR53:OP[4:0]). When loopback is enabled, the default RON drive mode described in the loopback function section is used. When loopback is disabled, the pin is set to termination mode or high-impedance mode according to MR36:OP[2:0].

Symbol	Type	Function
LBDQS	Output	Loopback Data Strobe: Single-ended strobe signal; rising edge aligned with loopback data edge, falling edge aligned with data center. When loopback mode is enabled, the default RON driver mode as described in the Loopback Function section is used. When disabled, the pin is set to termination or high impedance according to MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No connect: No internal electrical connection.
V_{DDQ}	Power Supply	DQ Power: 1.1 V
V_{DD}	Power Supply	Power Supply: 1.1 V
V_{SS}	Power Supply	Ground
V_{PP}	Power Supply	DRAM Activation Power: 1.8 V
ZQ	Reference	Reference pin for ZQ calibration. This pin is connected to an external 240 Ω resistor (RZQ) which is connected to VSS.

3. AC and DC Operating Conditions

3.1 Absolute Maximum Ratings

Table 3-1 DC Absolute Maximum Ratings

Symbol	Parameter	Max	Unit	Notes
VDD	VDD pin voltage relative to VSS	-0.3~ 1.4	V	1,3
VDDQ	VDDQ pin voltage relative to VSS	-0.3~ 1.4	V	1,3
VPP	VPP pin voltage relative to VSS	-0.3~ 2.1	V	4
VIN , VOUT	Any pin voltage relative to VSS	-0.3~ 1.4	V	1,3,5
TSTG	Storage temperature	-55 to +100	°C	1,2

Note 1: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect reliability.
Note 2: Storage temperature refers to the case surface temperature at the top/center area of the DRAM device. For specific measurement conditions, refer to JESD51-2 standard. Note 3: The voltage difference between VDD and VDDQ must always be kept within 300 mV.
Note 4: VPP voltage must always be equal to or greater than the maximum of VDD and VDDQ.
Note 5: The overshoot region above 1.5V is specified in Sections 4.3.5 and 4.3.6.

3.2 DC Operating Conditions

Table 3-2 DC Operating Conditions

Symbol	Parameter	Low-frequency voltage specification frequency: DC to 2 MHz				Z(f) specification frequency: 2 MHz to 10 MHz		Z(f) specification frequency: 20 MHz		Notes
		Min	Typ	Max	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067(-3%)	1.1	1.166(+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	I/O Supply Voltage	1.067(-3%)	1.1	1.166(+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	VPP Supply Voltage	1.746(-3%)	1.8	1.908(+6%)	V	10	mOhm	20	mOhm	3

Note 1: The voltage difference between VDD and VDDQ must always be kept within 300mV.
Note 2: AC parameters are measured with VDD and VDDQ shorted together.
Note 3: This includes all voltage noise from DC to 2MHz at the DRAM package solder balls.
Note 4: Z(f) is defined for all pins within each voltage domain. Z(f) does not include the DRAM package and silicon die.

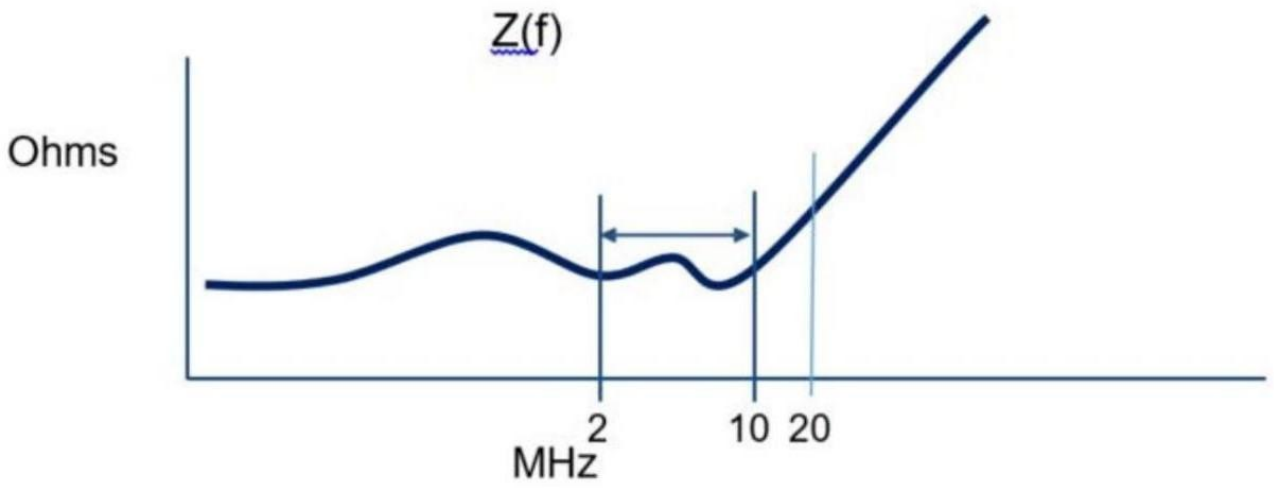


Figure 3-1 Impedance Profile/Z(f) Curve at the DRAM Package Ball (Excluding DRAM Component)

Figure 3-2 shows a simplified electrical system load model of Z(F) with a generic frequency response. Resistance and inductance can be scaled to generalize the specification response to DRAM pins.

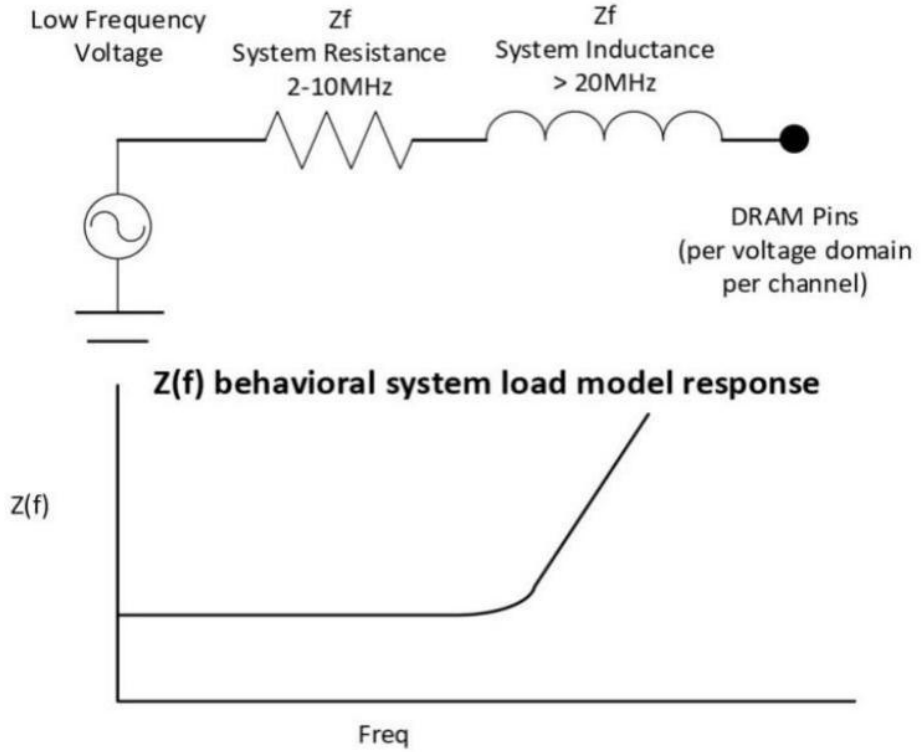


Figure 3-2 Simplified Z(f) Electrical Model and Frequency Response of PDN

Note: This is a model of the power distribution network (PDN) at the DRAM pin location, excluding the DRAM component.

3.3 DRAM Component Operating Temperature Range

Table 3-3 DC Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit: °C)		Unit	Note
		Min	Max		
Toper_normal	Normal Operating Temperature Range	0	85	NT	1,2,3,4
Toper_extended	Extended Operating Temperature Range	85	95	XT	1,2,3,4,5

Note 1: All operating temperature symbols, ranges, and abbreviations refer to JESD402-1 standard.
Note 2: Operating temperature refers to the DRAM center/top case surface temperature.
Measurement conditions refer to JESD51-2 standard. Note 3: All DDR5 SDRAM must
operate within the NT and XT temperature ranges.
Note 4: When the operating temperature exceeds 85°C, the host must provide refresh mode control corresponding to the extended temperature range.
Note 5: The operating temperature of 3DS must be derated according to the following formula based on the number of DRAM die: [TOPER – (2.5°C × log2N)], where N is the number of stacked die.

4. AC and DC Input Measurement Levels

This section defines the voltage tolerance limits of input signals and AC/DC logic input levels to ensure normal operation of DDR5 SDRAM.

- Reference CA Overshoot and Undershoot Specifications
- Reference CA Receive Voltage and Timing
- Reference Input Clock Jitter Specification
- Reference Differential Input Clock (CK_t, CK_c) Crossing Point Voltage (VIX)
- Reference Differential Input Clock Voltage Sensitivity
- Reference Receiver Data Quality Signal Jitter Sensitivity
- Reference Receiver DQS Voltage Sensitivity (page 21)
- Reference Differential Data Strobe (DQS_t, DQS_c) Input Crossing Point Voltage (VIX)
- Reference Receiver DQ Voltage Sensitivity
- Reference Receiver Stressed Eye Diagram
- Reference Connectivity Test Mode - Input Level and Timing Requirements

4.1 CA Receive Voltage and Timing

The following example assumes internal VREF for CA. If VREF is external, specifications will be adjusted accordingly. The command and address (CA) signals, including the CS input receiver voltage and timing tolerance mask, are shown in Figure 4-1. All CA and CS signals use the same tolerance mask and operate in single data rate mode.

The CA input receiver voltage and timing tolerance mask shown in Figure 4-1 applies to all CA pins. The receiver mask

(Rx Mask) defines the region that input signals must avoid to ensure the DRAM input receiver can successfully capture valid input signals; this region is not the valid data eye.

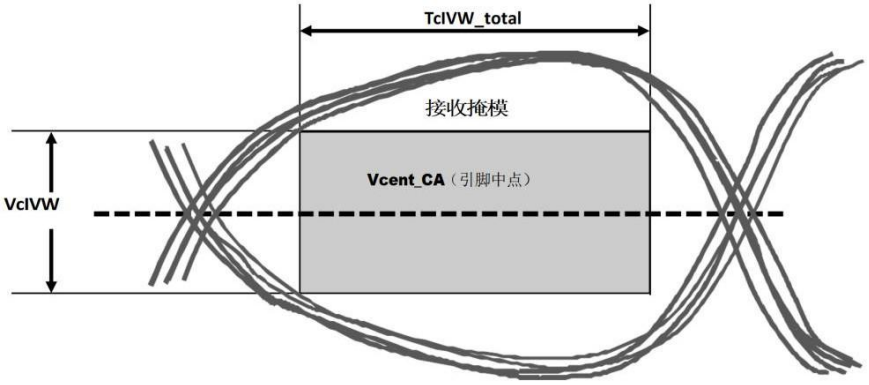


Figure 4-1 CA Receiver (Rx) Mask

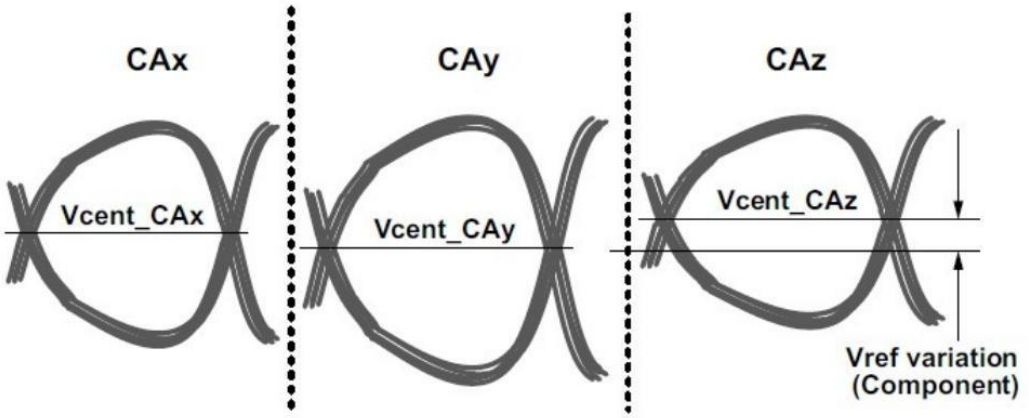


Figure 4-2 Pin VREFCA Voltage Variation

Vcent_CA (pin midpoint) is defined as the midpoint between the maximum and minimum Vcent_CA voltage levels across all CA and CS pins of a given DRAM device. Each CA Vcent level is defined by the center (i.e., widest opening) of the cumulative data input eye diagram shown in Figure 4-3. This explicitly requires that any DRAM device level variation must be taken into account in the DRAM CA receiver mask. The device-level VREF will be set by the system to compensate for Ron and ODT settings.

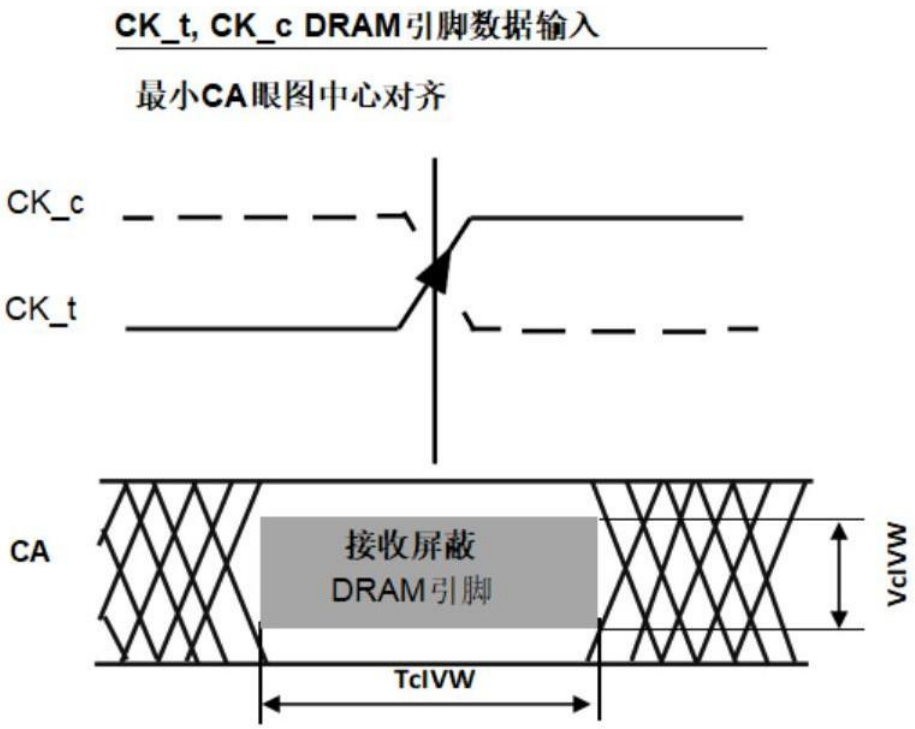


Figure 4-3 CA Timing on DRAM Pins

The TcIVW of all CA signals is defined as the crossing point of CK_t/CK_c at the DRAM pins.

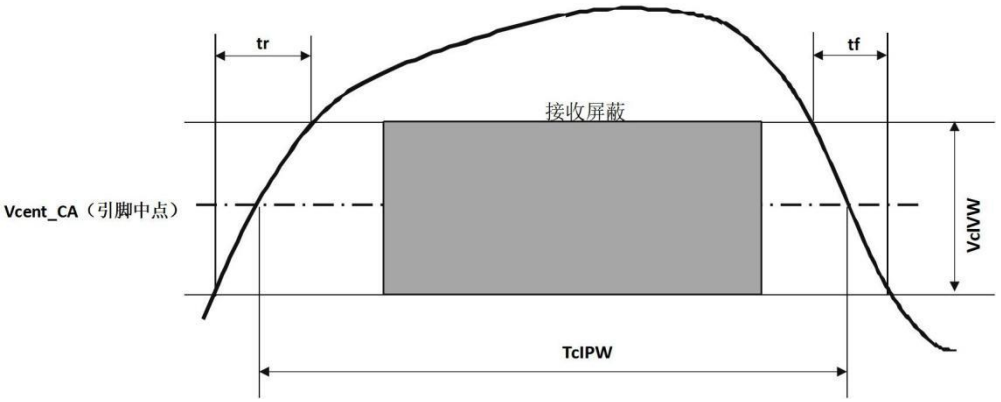


Figure 4-4 CA TcIPW and SRIN_cIVW Definition (per Input Pulse)

Note 1 SRIN_cIVW = VcIVW_Total / (Tr or Tf); the signal must maintain monotonicity within the Tr and Tf range.

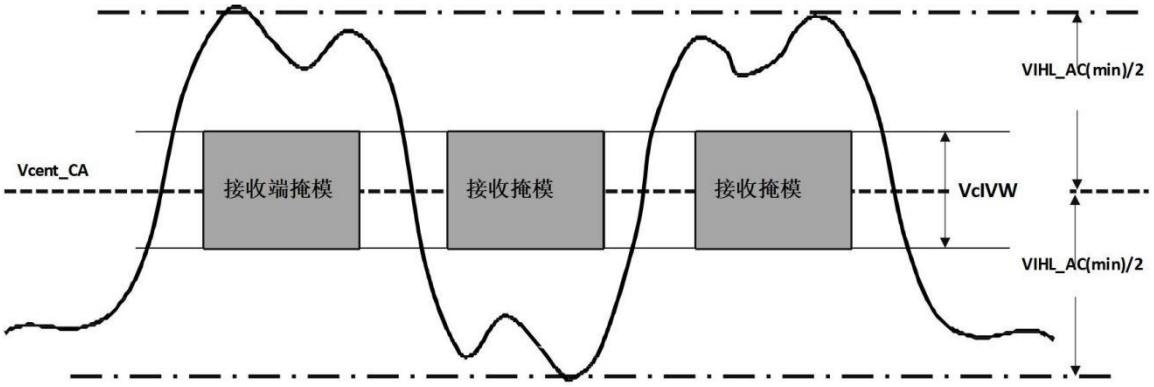


Figure 4-5 CA VIHL_AC Definition (per Input Pulse)

Table 4-1 DRAM CA and CS Parameter Values for DDR5-4800/5600/6400

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Receiver mask voltage - peak-to-peak	VciVW	-	130	-	110	-	95	mV	1,2,4
Receiver timing window	TcIVW	-	0.2	-	0.2	-	0.2	UI*	1,2,3,4,8
CA input differential voltage amplitude	VIHL_AC	150	-	125	-	115	-	mV	7
CA input pulse width	TcIPW	0.58	-	0.58	-	0.58	-	UI*	5,8
Input slew rate beyond VcIVW	SRIN_cIVW	1	7	1	7	1	7	V/ns	6

Note 1: Includes voltage and temperature drift of pin CA receiver mask voltage and timing parameters.
Note 2: The total receiver mask voltage VcIVW (maximum) must be centered around Vcent_CA (pin midpoint). Note 3: Total timing window for differential CA to CK jitter at VcIVW voltage level.
Note 4: The defined range covers the CA internal VREF range. The receive mask voltage at the pin must fall within the internal VREF CA range, regardless of the input signal common mode. Note 5: CA minimum input pulse width is defined only at Vcent_CA (pin midpoint).
Note 6: Input slew rate exceeds the VcIVW mask, which is centered at Vcent_CA (pin midpoint). Note 7: When no level transition occurs, VIHL_AC does not need to be satisfied.
Note 8: UI = tCK (average) minimum

4.2 Input Clock Jitter Specifications

4.2.1 Overview

The clock signal is driven to the DRAM by the RCD of the L/RDIMM module or by the host of the U/SODIMM module (Figure 4-6).

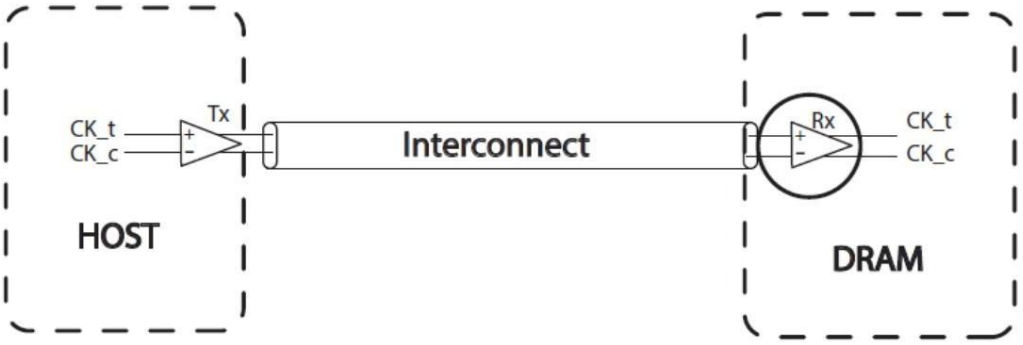


Figure 4-6 Host Driving Clock Signal to DRAM

4.2.2 DRAM Input Clock Jitter Specifications

Random jitter (Rj) is random jitter that follows a Gaussian distribution. Deterministic jitter (Dj) has an upper bound. Violating the minimum/maximum jitter values on the input clock may cause the DDR5 SDRAM device to function abnormally.

Table 4-2 DDR5-4800/5600/6400 DRAM Input Clock Jitter Specifications

BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; Tj = Total Jitter; pp = peak-to-peak

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DRAM reference clock frequency	tCK	0.9999*f0	1.0001*f0	0.9999*f0	1.0001*f0	0.9999*f0	1.0001×f0	MHz	1.11
Duty cycle error	tCK_duty_cycle_UI_error	-	0.05	-	0.05	-	TBD	UI	1,4,11
Rj (1-UI) jitter RMS value	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	TBD	UI (RMS)	3,5,11
Dj (peak-to-peak) 1-UI jitter	tCK_1UI_Dj_NoJitter	-	0.030	-	0.030	-	TBD	UI	3,6,11
1-UI total jitter (Tj) value	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	TBD	UI	3,6,11
N-UI jitter RMS value where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	-	TBD	UI (RMS)	3,7,11
Dj pp value (N=2,3)	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	-	TBD	UI	3,7,11
N-UI jitter Tj value where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	-	TBD	UI	3,8,11
N-UI Jitter Rj RMS value, N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI (RMS)	3,9,11,12
N-UI Jitter Dj pp value, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ , where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	3,10,11,12
N-UI jitter Tj value, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	3,10,11,12

Note 1: f0 = data rate / 2, e.g., if data rate is 3200 MT/s, then f0 = 1600 MHz

Note 2: Rising/falling slew rates (V/nsec) are measured over the range from +100 mV to -100 mV of the reference clock differential output.

Note 3: When there is no socket in the transmitter measurement setup, in many cases even if all transmitter channels are in transmit mode, the effect of crosstalk is not significant or can be estimated within a tolerable error range.

When a socket is present (e.g., the DUT is a DRAM device), the effect of crosstalk may be significant. To minimize the impact of crosstalk on measurement results, adjacent channels near the DUT channel can be turned off (transmitting DC signals) while the remaining transmitter channels send signal patterns to their corresponding receivers, thereby exciting the real on-chip noise generated by device switching. Note: When one of the deterministic jitter (Dj) and random jitter (Rj) specifications is met while the other is not, a signal integrity analysis should be performed to determine link feasibility.

Note 4: Duty cycle error is defined as the absolute difference between the average of all UIs and the average of odd UIs; its absolute value is equivalent to the absolute difference between the average of all UIs and the average of all even UIs.

Note 5: The Rj RMS value is the 1-UI jitter (without BUJ correction), but with on-chip system noise present. This extraction must be performed after software DCC correction.

Note 6: The Dj pp value is the 1-UI jitter (after software-assisted DCC processing). No BUJ correction is used, but on-chip system noise is present.

Djdd value after dual-Dirac fitting

Note 7: Rj is the RMS value of N-UI jitter without BUJ processing, but with on-chip system noise. Evaluation condition: 1 < N < 4. This extraction shall be performed after DCD software correction.

Note 8: Dj is the peak-to-peak (pp) value of N-UI jitter without BUJ, but with on-chip system noise. Evaluation condition: 1 < N < 4. Dj refers to the Djdd value after dual-Dirac fitting with DCD software correction.

Note 9: Rj is the RMS value of N-UI jitter without BUJ processing, but with on-chip system noise. The evaluation is based on the condition 3 < N < 31. This extraction shall be performed after

DCD software correction

Note 10: Dj is the peak-to-peak (pp) value of N-UI jitter without BUJ, but with on-chip system noise. Evaluation condition: 1 < N < 31. Dj represents the Djdd value from dual-Dirac fitting, obtained after DCD software correction.

Note 11: The characterization method for these parameters will be described in a future revision.

Note 12: If the clock meets the total jitter Tj at 1E-16 BER, the specification is considered satisfied, and individual Rj and Dj components are optional. Tj is defined as: Tj = Dj + 16.2 × Rj at 1E-16 BER.

4.3 Differential Input Clock (CK_t, CK_c) Crossing Point Voltage (VIX)

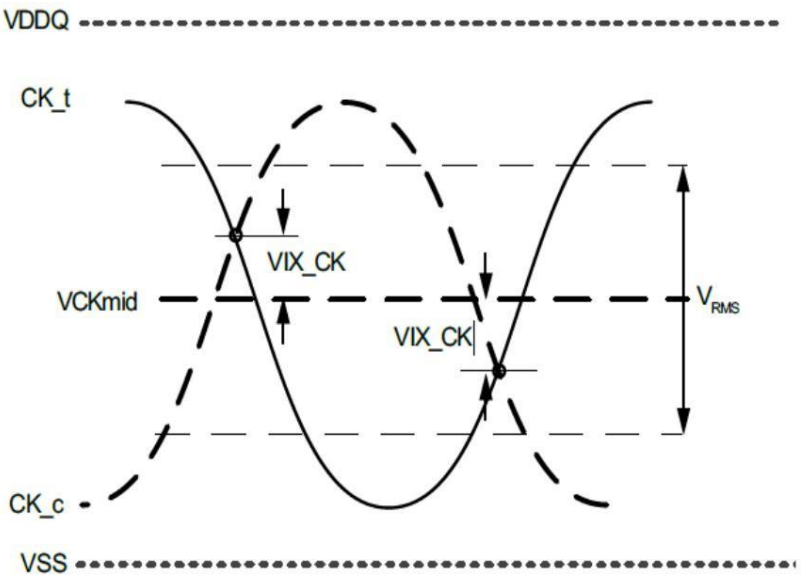


Figure 4-7 VIX Definition (CK)

Table 4-3 Differential Input Clock Crossing Point (VIX)

Parameter	Symbol	DDR5-4800/5600/6400		Unit	Notes
		Min	Max		
Differential input clock crossover voltage ratio	VIX_CK_Ratio	-	50	%	1,2,3
Note 1: VIX_CK voltage is referenced to VCKmid (mean) = (CK_t voltage + CK_c voltage)/2, where the mean is averaged over 8UI; Note 2: VIX_CK_Ratio = (|VIX_CK|/|VRMS|)*100%, where VRMS = RMS(CK_t voltage - CK_c voltage); Note 3: Applicable only when CK_t and CK_c are both in transition state;					

4.4 Differential input clock voltage sensitivity

The differential input clock voltage sensitivity test provides a method for evaluating the receiver's sensitivity to the clock by varying the input voltage under conditions free of intersymbol interference (ISI), jitter (Rj, Dj, DCD), and crosstalk noise. This specification defines the receiver voltage sensitivity requirements. The input swing provided by the system to the DRAM must be greater than the DRAM receiver's requirement at the specified bit error rate (BER).

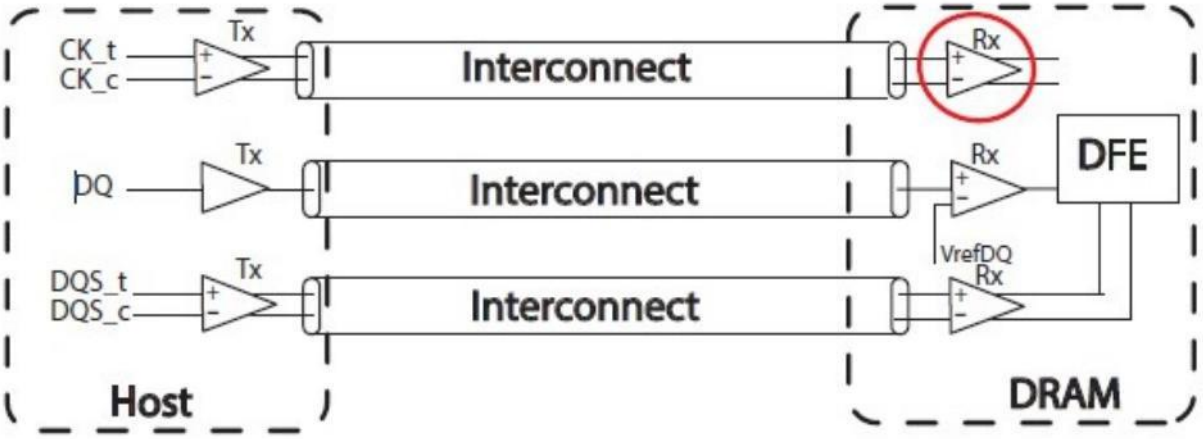


Figure 4-8 DDR5 Memory Interconnect Example

4.4.1 Differential input clock voltage sensitivity parameters

The definition and measurement method of VRx_CK for the differential input clocks (CK_t, CK_c) are shown in Table 4-4. The clock receiver must meet

the minimum bit error rate (BER) requirement of DDR5.

Table 4-4 Differential Input Clock Voltage Sensitivity Parameters for DDR5-4800/5600/6400

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input Clock Voltage Sensitivity (Differential pp) pp)	VRx_CK	-	160	-	120	-	100(*120)	mV	1,2
Note: Refer to Section 7.2.3 for the minimum BER requirement of DDR5;									

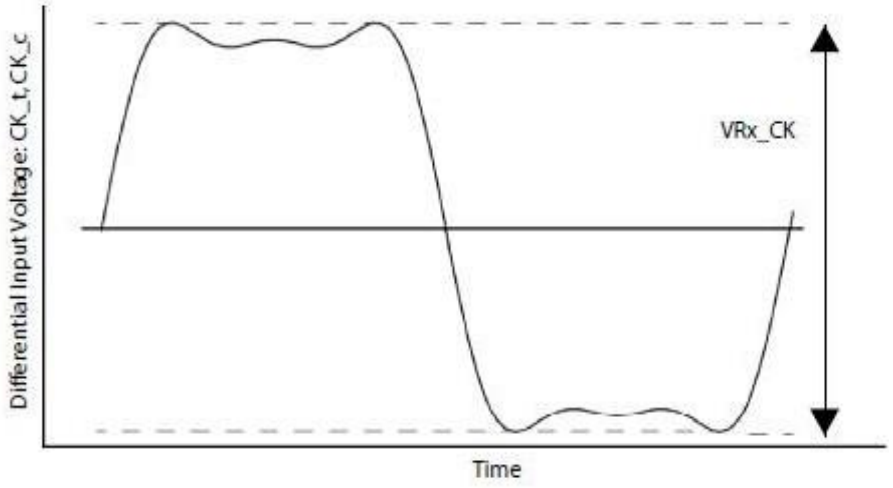


Figure 4-9 VRx_CK

4.4.2 Differential input clock voltage sensitivity parameters

Table 4-5 Differential Input Clock Voltage Sensitivity Parameters for DDR5-4800/5600/6400

Parameter	Parameter	DDR5-4800/5600/6400	Notes
VIHdiffCK	Differential input high level measurement (CK_t, CK_c)	0.75 × Vdiffpp	1,2
VILdiffCK	Differential input low level (CK_t, CK_c)	0.25 × Vdiffpp	1,2
Note 1: Vdiffpk-pk is defined in Figure 4-10; Note 2: Vdiffpk-pk is the mean of the high voltage minus the mean of the low voltage during TBD number of samples. Note 3: All parameters are defined over the full clock common-mode voltage range.			

4.4.3 Differential input clock voltage sensitivity parameters

Input slew rate definition and measurement method for differential signals (CK_t, CK_c) is shown in Figure 4-10

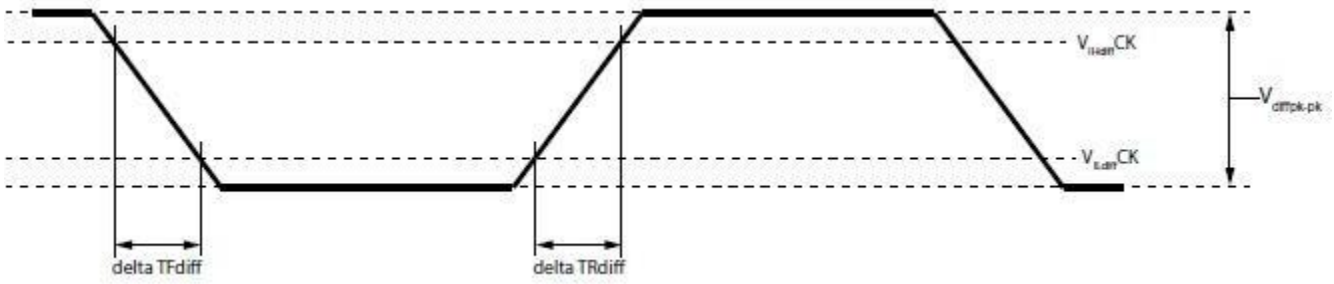


Figure 4-10: Differential Input Slew Rate Definition for CK_t and CK_c

Table 4-6: Differential Input Slew Rate Definition (CK_t, CK_c)

Parameter	Measurement		Definition	Notes
	Source	To		
Rising edge differential input slew rate (CK_t - CK_c)	VILdiffCK	VIH diff CK	(VIHdiffCK - VILdiffCK) /deltaTRdiff	
Falling edge differential input slew rate (CK_t - CK_c)	VIHdiffCK	VIL diff CK	(VIHdiffCK - VILdiffCK) /deltaTFdiff	

Table 4-7 Differential Input Slew Rate for CK_t and CK_c in DDR5-4800/5600/6400 Modes

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Differential input slew rate for CK_t, CK_c	SRdiff_CK	2	14	2	30	2	30	V/ns	

4.5 Receiver DQS jitter sensitivity

The receiver DQS jitter sensitivity test provides a method for testing the receiver's sensitivity to clocks with applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded clock input, without adding jitter, noise, and crosstalk to the data. The receiver must pass the corresponding bit error ratio (BER) test without crosstalk or mutual coupling, and must also pass the test with applied DCD and Rj combinations.

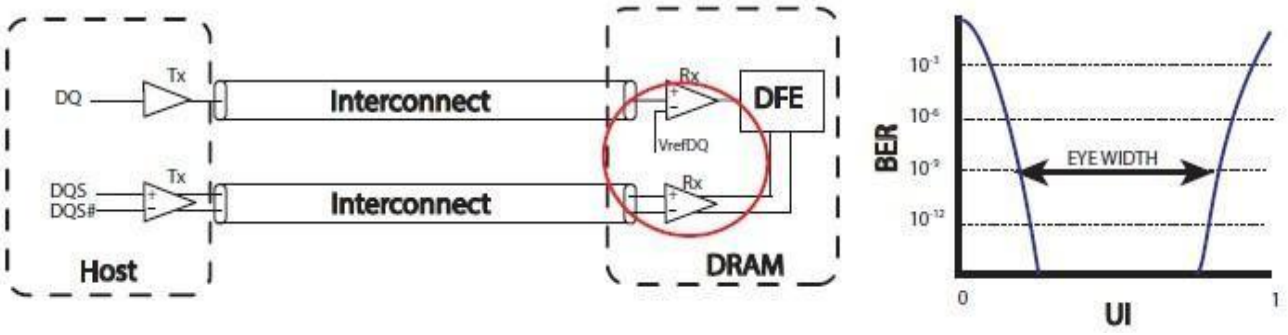


Figure 4-11 Forwarded clock pulse for SDRAM receiver jitter sensitivity test

4.5.1 Receiver data quality system jitter sensitivity specification

Table 4-7 provides the DDR5 DRAM receiver DQS jitter sensitivity specifications for the receiver operating at different data rates. These parameters are tested on a CTC2 card without receiver equalization. Additional DFE gain bias may be set.

Table 4-8 DDR5-4800/5600/6400 Receiver DQS Jitter Sensitivity Specification

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter]

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQ Timing Margin	tRx_DQ_tMargin	0.825	-	0.835	-	0.845	-	UI	1,2,3,8,9,10
Timing margin degradation relative to tRx_DQ_tMargin when DCD is injected into DQS	Δ tRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	-	0.06	UI	1,4,8,9,10
Timing width degradation relative to tRx_DQ _tMargin when Rj is injected into DQS	Δ tRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	-	0.09	UI	1,5,8,9,10
Timing margin degradation relative to tRx_DQ_tMargin, when both DCD and Rj are injected into DQS	Δ tRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	UI	1,2,6,8,9,10
Relative delay of any data channel DQS_t/DQS_c crossover delay	tRx_DQS2DQ	114	729	114	714	114	703	ps	1,7,8,9,10
Delay of any data channel relative to other data channels	tRx_DQ2DQ	-	50	-	50	-	50	ps	

Note 1: The verification method will be determined in a future ballot. 2UI is defined as 1tCK in this parameter.
Note 2: ΔtRx_DQ_tMargin_DQS_DCD, tRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS_DCD_Rj are allowed to relax by up to 5%, provided that tRx_DQ_tMargin exceeds the specification by 5% or more.
Note 3: DQ timing width – timing width of any data channel using a repeating pattern (see Note 4 for pattern details), measured at a bit error rate (BER) of E-9.
Note 4: Under BER=E-9, using a DCD-injected forward-strobed DQS, with a repeating no-ISI pattern, the ratio of the timing width degradation of any data channel to tRx_DQ_tMargin. The DCD amplitude is specified in the test conditions for receiver DQS jitter sensitivity testing. The test uses a clock-like pattern: repeating three '1's and three '0's.
Note 5: When using a repeating no-ISI pattern with only Rj injection, the timing width degradation magnitude (BER=E-9) measured on any data channel in the forwarded strobe DQS, relative to tRx_DQ_tMargin. The magnitude of Rj is specified under the receiver DQS jitter sensitivity test conditions.
Note 6: Under BER=E-9 condition, the ratio of the timing width degradation magnitude to tRx_DQ_tMargin for a forwarded strobe DQS data channel using a repeating no-ISI pattern with DCD and Rj injection. The specific values of DCD and Rj are specified in the receiver DQS jitter sensitivity test conditions.
Note 7: The delay of any data channel relative to the clock channel, measured at the end of the Tx-side channel. This parameter is the sum of the Tx-side data-clock mismatch effect and the transmission medium mismatch effect between Tx and Rx.
Note 8: All measurements are performed under BER=E-9 condition.
Note 9: This test should be performed after the DQS and DQ voltage sensitivity tests are completed and passed.
Note 10: The user may freely set the voltage swing and rise/fall rate of the clock pulse and DQ signals, provided that the specification requirements are met. In this test, the DQS and DQ input voltage swing and/or rise/fall rate may be adjusted, but must not exceed the specified limits.

4.5.2 Receiver DQS Jitter Sensitivity Test Conditions

Table 4-4 lists the amounts of duty cycle distortion (DCD) and/or random jitter (Rj) that must be applied to the transmitted pulse when measuring the receiver DQS jitter sensitivity parameters specified in Tables 4-4 and 4-9.

Table 4-9 DDR5-5600 Receiver DQS Jitter Sensitivity Test Conditions

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DCD applied to DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	UI	1,2,3,6,7, 10
Rj RMS applied to DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1,2,4,6,8, 10
DCD and Rj RMS applied to DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 0.0075UI Rj RMS	UI	1,2,5,6,7, 9,10

Note 1: When applying this specification, the memory channel is under stress, but the data inputs maintain large amplitude and no jitter or ISI is injected. The specified voltage values are at the receiver input pins. In this test, DQS and DQ input voltage swing and/or rise/fall rate may be adjusted without exceeding the specifications.
Note 2: The jitter response of the forwarded clock channel mainly depends on the input voltage, which is primarily limited by the bandwidth of the clock receiver. This revision does not separately specify input-amplitude-dependent jitter specifications; response characterization is performed only at specified clock amplitudes. The specified voltage values are at the receiver input pins.
Note 3: Multiple DCD values shall be tested to ensure compliance
within the maximum limits; Note 4: Multiple Rj values shall be
tested to ensure compliance within the maximum limits.
Note 5: Various combinations of DCD and Rj shall be tested to ensure they are within the maximum limits. The maximum timing margin degradation caused by these injected jitter values is specified in a separate table.
Note 6: Although DDR5 has burst traffic, currently available BERT equipment for this test does not support burst traffic mode. This parameter is tested using continuous clock pulses and continuous DQ signals. A clock pattern repeating 3 '1's and 3 '0's is used in the test.
Note 7: Duty cycle distortion (in UI DCD) applies to the forward DQS signal output from the BERT (UI).
Note 8: The RMS value of Rj (defined as edge jitter) is applied to the forward DQS output from the BERT (edge jitter RMS value expressed as a percentage of UI).
Note 9: Duty cycle distortion (expressed as UI DCD) and the RMS value of Rj (expressed as edge jitter) applied to the DQS input from the BERT output (edge jitter RMS value expressed as a percentage of UI).
Note 10: The user is free to set the voltage swing and slew rate of the strobe and DQ signals as long as they meet the specifications. The DQS and DQ input voltage swing and/or slew rate can be adjusted without exceeding the specifications.

4.6 Receiver DQ Voltage Sensitivity

4.6.1 Overview

The receiver data input voltage sensitivity test provides a method for testing the receiver's sensitivity to input voltage variations under conditions without intersymbol interference (ISI), jitter (Rj, Dj, DCD), and crosstalk noise.

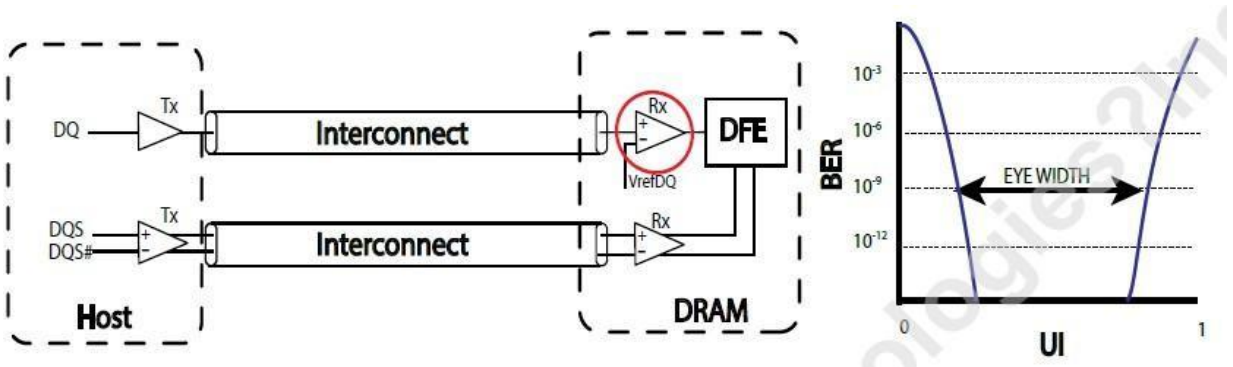


Figure 4-12 DDR5 Memory Interconnect Example

4.6.2 Receiver DQ Voltage Sensitivity Parameters

This section defines and measures the input single-ended voltage VRx_DQ. The receiver must meet the minimum bit error rate (BER) requirements of DDR5. When testing on the CTC2 card, these parameters are measured without setting additional gain or enabling receiver equalization.

Table 4-10 DDR5-5600 Receiver DQS Jitter Sensitivity Test Conditions

Parameter	Symbol	DDR5-4800/5600/6400		Unit	Notes
		Min	Max		
Minimum DQ receiver input voltage sensitivity (near Vref)	VRx_DQ	-	65/60/55	mV	1,2,3

Note 1: Refer to the minimum BER requirements for DDR5
Note 2: The verification methodology for this parameter will be described in a future ballot.
Note 3: It is recommended to use a clock pattern test mode, for example, repeating three '1's and three '0's.

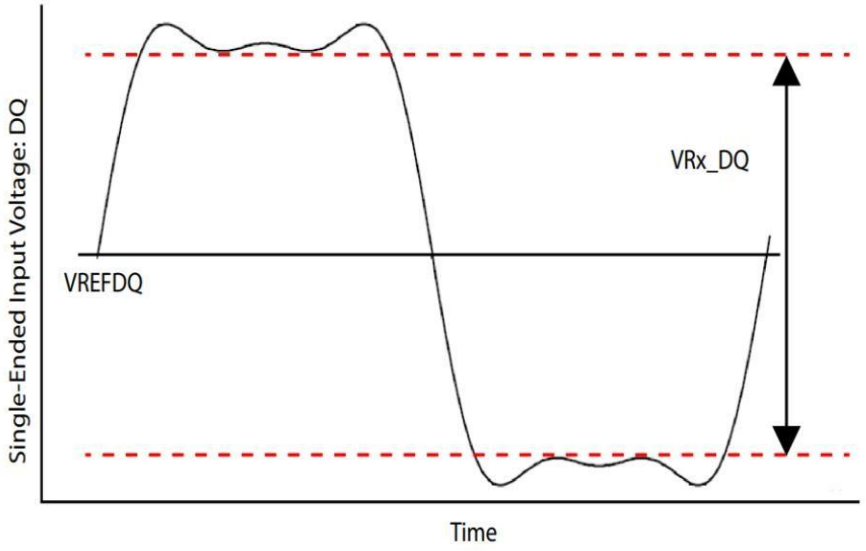


Figure 4-13 VRx_DQ

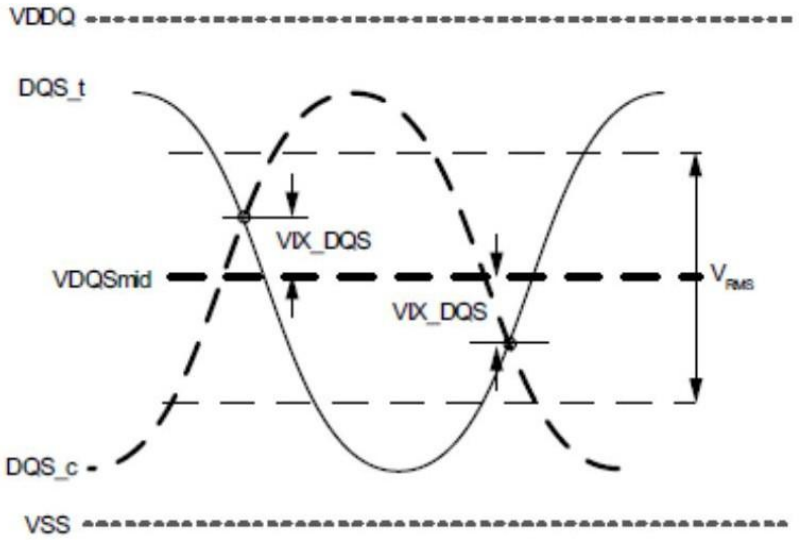


Figure 4-14 VIX Definition (DQS)

4.7 Differential Strobe Signal (DQS_t, DQS_c) Input Crossing Point Voltage (VIX)

Table 4-11 Differential Strobe Signal (DQS) Crossing Point Voltage (VIX)

Parameter	Symbol	DDR5-4800/5600/6400		Unit	Notes
		Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	%	1,2,3
Note 1: VIX_DQS voltage is referenced to VDQSmid (average) = (DQS_t voltage + DQS_c voltage) /2, where the average is taken over more than 8 UI; Note 2: VIX_DQS_Ratio = (|VIX_DQS| / |VRMS|)*100%, where VRMS = RMS(DQS_t voltage - DQS_c voltage); Note 3: Applicable only when DQS_t and DQS_c are both in transition (including preamble);					

4.8 Receiver DQS voltage sensitivity

4.8.1 Overview

The receiver DQS (data strobe) input voltage sensitivity test provides a method to detect the receiver's sensitivity to input voltage changes under conditions without inter-symbol interference (ISI), jitter (Rj, Dj, DCD), and crosstalk noise.

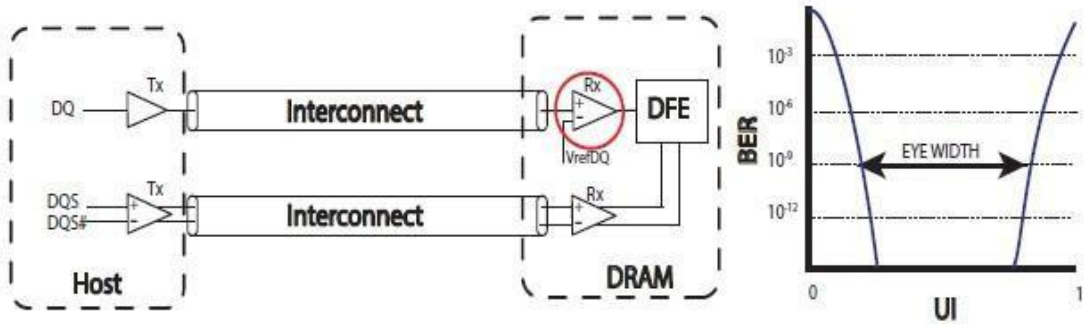


Figure 4-15 DDR5 Memory Interconnect Example

4.8.2 Receiver DQS Voltage Sensitivity Parameters

The definition and measurement method of the input differential voltage (DQS_t, DQS_c) VRx_DQS are shown in Table 4-12. The receiver must meet the minimum bit error rate (BER) requirements of DDR5. When testing these parameters on a CTC2 card, no additional gain is set and the receiver equalization is not enabled.

Table 4-12 Rx DQ Input Voltage Sensitivity Parameters for DDR5-4800/5600/6400

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-4800/5600/6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS receiver input voltage sensitivity (differential peak-to-peak)	VRx_DQS	-	100	-	90	-	83	mV	1,2,3
Note 1: Refer to the minimum BER requirement for DDR5; Note 2: The verification method for this parameter will be specified in a future ballot; Note 3: Test using clock pattern, i.e., repeating 3 ones and 3 zeros.									

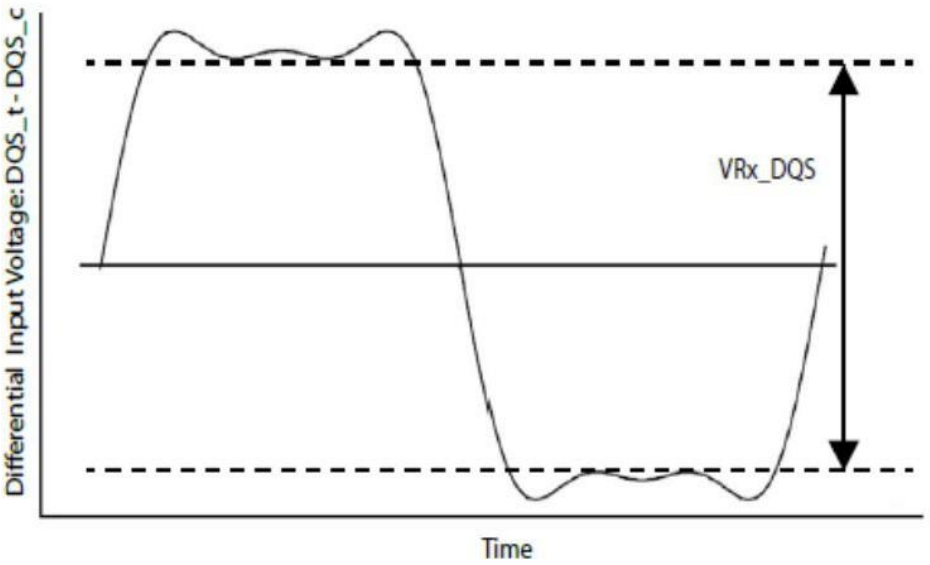


Figure 4-16 VRx_DQS

4.8.3 DQS Differential Input Level

Table 18: DQS Differential Input Level (DQS_t, DQS_c) for DDR5-4800/5600/6400

Source	Symbol	DDR5-4800/5600/6400	Notes
VIHdiffDQS	Differential Input High Level Measurement (DQS_t, DQS_c)	0.75 × Vdiffpk-pk	1,2,3
Differential Input Low Level Measurement (DQS_t, DQS_c)	Differential Input Low Level Measurement (DQS_t, DQS_c)	0.25 × Vdiffpk-pk	1,2,3
Note 1: Vdiffpk-pk is defined in Figure 4-17; Note 2: Vdiffpk-pk is the average high voltage minus average low voltage over TBD sampling periods; Note 3: All parameters are defined over the entire clock common-mode voltage range;			

4.8.4 Differential input slew rate applies to DQS_t, DQS_c

The definition and measurement method of input slew rate for differential signals are shown in Figure 4-17 below.

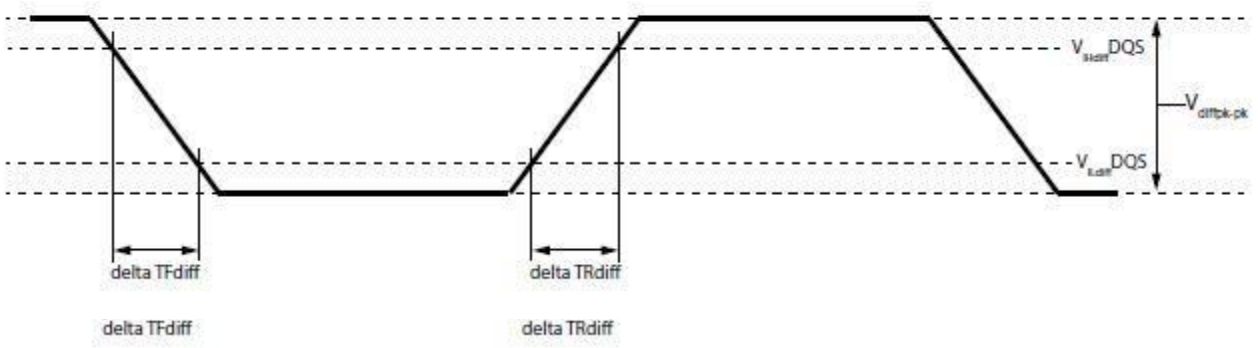


Figure 4-17 Differential Input Slew Rate Definition for DQS_t and DQS_c

Table 4-14 Differential Input Slew Rate Definition for DQS_t and DQS_c

Parameter	Measurement		Unit	Notes
	From	To		
Rising Edge Differential Input Slew Rate (DQS_t, DQS_c)	$V_{ILdiffDQS}$	$V_{IHdiffDQS}$	($V_{IHdiffDQS}$-$V_{ILdiffDQS}$)/delta TR_{diff}	1,2,3
Falling Edge Differential Input Slew Rate (DQS_t, DQS_c)	$V_{IHdiffDQS}$	$V_{ILdiffDQS}$	($V_{IHdiffDQS}$-$V_{ILdiffDQS}$)/delta TF_{diff}	1,2,3

Table 4-15 DDR5-5600 Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	DDR5-4800/5600/6400		Unit	Notes
		Min	Max		
Differential input slew rate for DQS_t and DQS_c	SRIdiff_DQS	TBD	TBD	mV	1
Note 1: Applicable only when DQS_t and DQS_c transition simultaneously.					

4.9 Rx Stressed Eye Diagram

The stressed eye test provides a method to apply appropriate stress to the DRAM receiver by combining intersymbol interference (including loss and reflection), jitter (Rj, Dj, DCD), and crosstalk noise. When an equivalent stressed eye is applied through a combination of ISI, jitter, and crosstalk, the receiver must meet the corresponding bit error rate (BER) threshold.

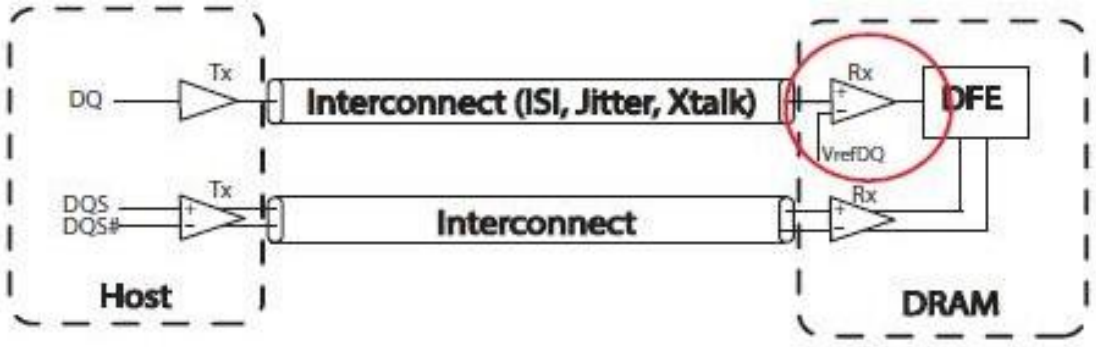


Figure 4- 18 Example of Receiver Stress Test Setup with ISI, Jitter, and Crosstalk

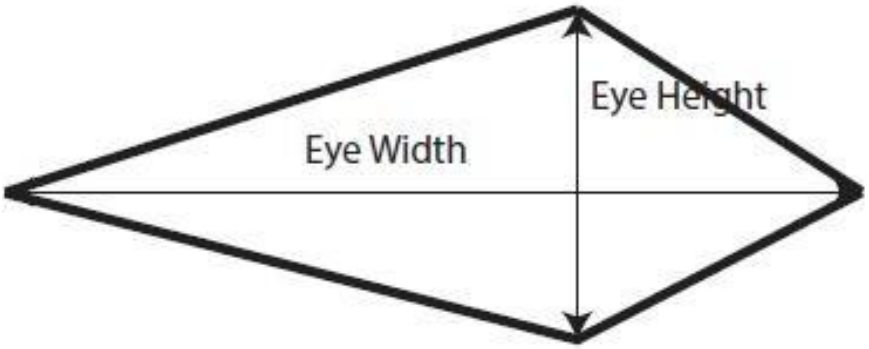


Figure 4-19 Receiver Stressed Eye Height and Width Example

4.9.1 DDR5 Receiver Stressed Eye Test Parameters

Table 4-16 DDR5-5600 Receiver Stressed Eye Test Conditions

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p=Peak-to-Peak]

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Stressed eye height for golden reference lane 1	RxEH_StressedEye_GoldenRefLane1	-	70	-	60	-	57.5	mV	1,2,3,4,5, 6,7,8,9,10
Stressed eye width of golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.235	-	0.230	UI	1,2,3,4,5, 6,7,8,9,10
Swing stressed data eye applied to meet the above requirements	Vswing_Stressed_Eye_Golden_Ref_Channel_ 1	-	600	-	600	-	600	mV	1,2
Sine jitter injected at 200 MHz to meet the above data eye requirements	Sj_Stressed_Eye_Golden_Ref_Channel_1	-	0.45	-	0.45	-	0.45	UI p-p	1,2
Injected random broadband noise (10 MHz to 1 GHz) Injected random broadband jitter (10 MHz–1 GHz)	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise (PRBS23) or Injected 2.1 GHz Voltage Noise	Vnoise_Stressed_Eye_Golden_Ref_Channel_ 1	0	125	0	125	0	125	mV pk-pk	1,2
Golden Reference Channel 1 Characteristics (measured at TBD	Golden Reference Channel 1 Characteristics	TBD		TBD	TBD	TBD	TBD	dB	3

Note 1: The minimum bit error rate (BER) at the receiver slicer (after application of equalization) for the stressed eye must be 1×10^{-16} or better. The eye is verified by measuring to a BER of 1×10^{-9} and extrapolating to a BER of 1×10^{-16}.
1×10^{-9} and extrapolating to a BER of 1×10^{-16} to verify the eye shape;
Note 2: These parameters apply to the defined golden reference channel; specific parameters are TBD;
Note 3: DFE tap range limits apply: the sum of the absolute values of Tap-2, Tap-3, and Tap-4 must be less than 60 mV (|Tap-2| + |Tap-3| + |Tap-4| < 60 mV); Note 4: Evaluated under no DC supply voltage drift conditions;
Note 5: Evaluated under no temperature drift conditions;

4.10 Connectivity Test Mode - Input Level and Timing Requirements

During CT mode, the input levels are defined as follows:

- TEN pin: CMOS rail-to-rail input, AC high level is 80% of VDDQ, low level is 20% of VDDQ.
- CS_n: CMOS rail-to-rail input, AC high level is 80% of VDDQ, low level is 20% of VDDQ.
- Test input pins: CMOS rail-to-rail input, AC high level is 80% of VDDQ, low level is 20% of VDDQ.
- RESET_n: CMOS rail-to-rail input, AC high level is 80% of VDDQ, low level is 20% of VDDQ. Before the TEN pin is asserted, all power supplies must be valid and stable.

When the TEN pin is driven high, the CK_t and CK_c signals are ignored, and the DDR5 memory device enters CT mode after tCT_Enable time. In CT mode, no refresh operations of the memory array occur, whether externally triggered auto-refresh or internally triggered self-refresh.

The TEN pin can be asserted after the DRAM completes power-up, after RESET_n is de-asserted and the wait time has elapsed, and before the clock signals (CK_t, CK_c) are started.

In CT mode, the TEN pin can be de-asserted at any time. Upon exiting CT mode, the state of the DDR5 memory device is unknown, and the integrity of the original memory array contents cannot be guaranteed; therefore, a reset initialization sequence must be executed.

When the test input is applied to the corresponding input pin, all output signals will become stable within tCT_valid cycles while keeping TEN input high and CS_n input low.

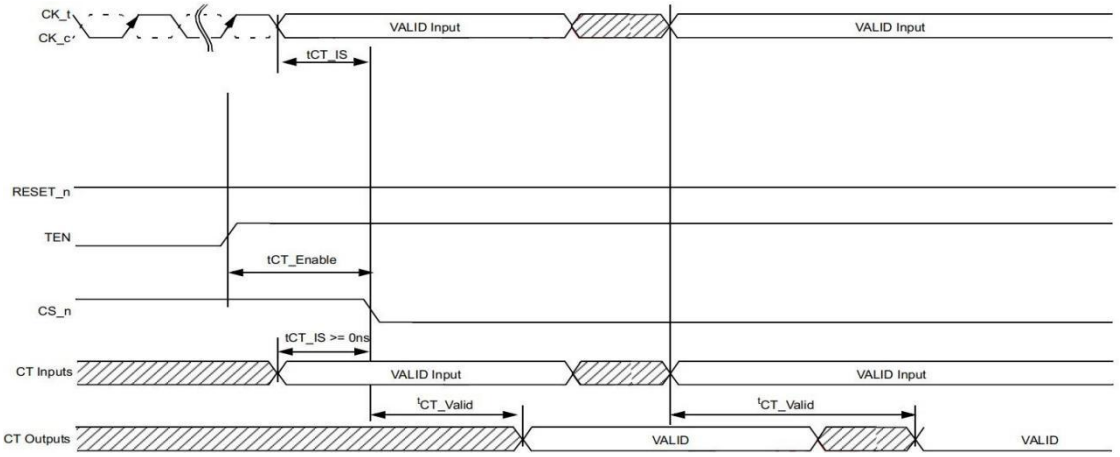


Figure 4-20 Connectivity Test (CT) Mode Timing Diagram

Table 4-17 Connectivity Test (CT) Mode AC Parameters

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_valid	-	200	ns

4.10.1 Connectivity Test (CT) Mode Input Levels

In connectivity test mode, the DDR5 SDRAM input signals shall use the following input parameters.

Table 4-18 CMOS Rail-to-Rail Input Levels for TEN, CS_n, and Test Inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input Signal Fall Time	tF_input_TEN	-	10	ns	
TEN Input Signal Rise Time	tR_input_TEN	-	10	ns	
Note 1: Overshoot may occur. It should be limited by the absolute maximum DC rating. Note 2: Undershoot may occur. Its magnitude should be limited by the absolute maximum DC rating.					

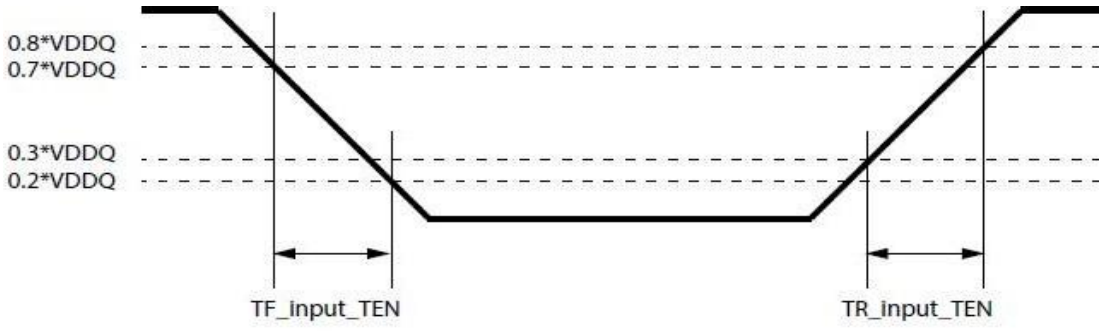


Figure 4-21 TEN Input Slew Rate Definition

4.10.2 CMOS Rail-to-Rail Input Levels (RESET_n)

Table 4-19 CMOS Rail-to-Rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	Notes
AC Input High Voltage	VIH(AC)_RESET	0.8 * VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7 * VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3 * VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2 * VDDQ	V	6
Rise Time	TR_RESET	-	1.0	ns	
Reset Pulse Width	tPW_RESET	1.0	-	ns	3,4

Note 1: After RESET_n is driven low, its voltage must remain below VIL(DC)_RESET during tPW_RESET; otherwise, the SDRAM may not reset.
Note 2: Once RESET_n is driven high, its voltage level must be maintained above VIH(DC)_RESET; otherwise, SDRAM operation is not guaranteed until a reset is performed by driving RESET_n low.
Note 3: A reset operation will result in loss of data contents.
Note 4: This definition applies only to the "reset procedure while power is stable."
Note 5: Overshoot may occur. It must be limited by the
absolute maximum DC rating. Note 6: Undershoot may occur.
It must be limited by the absolute maximum DC rating.

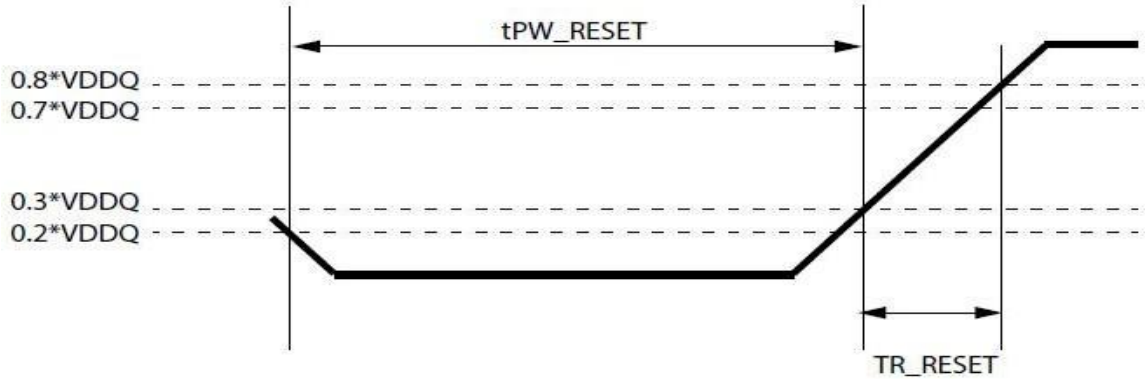


Figure 4-22 RESET_n Input Slew Rate Definition

5. AC and DC Output Measurement Levels and Timing

5.1 DC Electrical Characteristics of DQS and DQ Output Drivers

DDR5 drivers support two different RON values. These RON values are referred to as strong mode (low RON) and weak mode (high RON). The output buffer functional diagram is shown in Figure 5-1.

The output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

With RONPd turned off:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$

With RONPu off:

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$

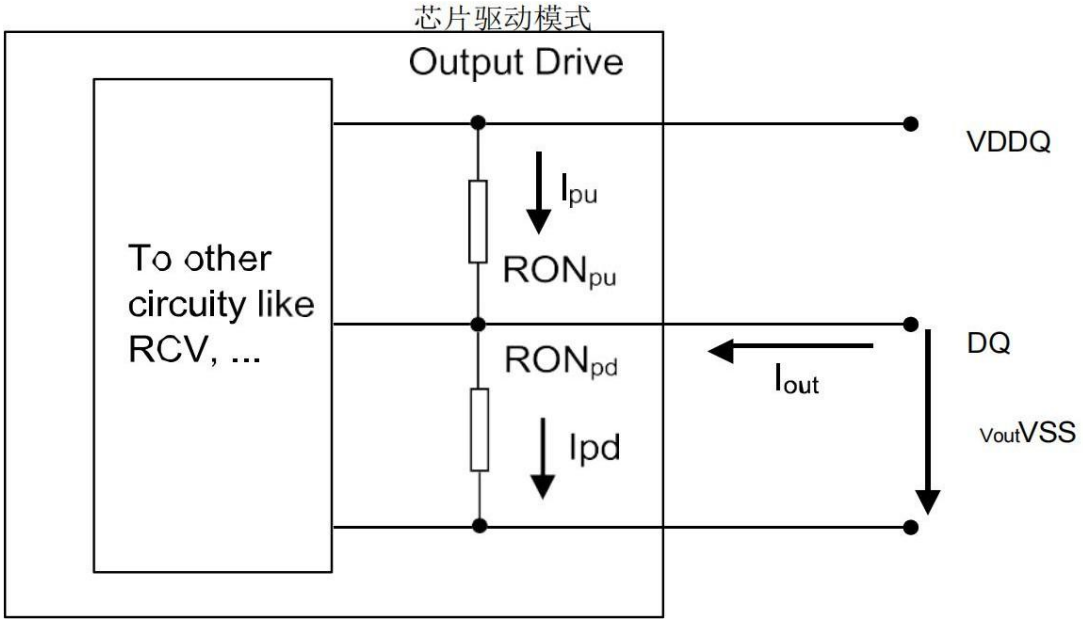


Figure 5-1 DQS and DQ Output Driver DC Electrical Characteristics

Table 5-1 Output Driver DC Electrical Characteristics

Assuming RZQ = 240 Ω, after correct ZQ calibration over the full operating temperature range:

RONNOM	Resistor	Vout	Min	Nominal	Max	Unit	Note
34Ω	RON34Pd	DC voltage = 0.5*VDDQ	0.8	1.0	1.1	RZQ/7	1,2
		VOMdc=0.8*VDDQ	0.9	1.0	1.1	RZQ/7	1,2
		VOHdc= 0.95*VDDQ	0.9	1.0	1.25	RZQ/7	1,2
	RON34Pu	VOLdc=0.5*VDDQ	0.9	1.0	1.25	RZQ/7	1,2
		VOMdc=0.8*VDDQ	0.9	1.0	1.1	RZQ/7	1,2
		VOHdc=0.95*VDDQ	0.8	1.0	1.25	RZQ/7	1,2
48Ω	RON48Pd	DC voltage = 0.5*VDDQ	0.8	1.0	1.1	RZQ/5	1,2
		VOMdc=0.8*VDDQ	0.9	1.0	1.1	RZQ/5	1,2
		VOHdc=0.95*VDDQ	0.9	1.0	1.25	RZQ/5	1,2
	RON48Pu	VOLdc=0.5*VDDQ	0.9	1.0	1.25	RZQ/5	1.2
		VOMdc=0.8*VDDQ	0.9	1.0	1.1	RZQ/5	1,2
		VOHdc=0.95*VDDQ	0.8	1.0	1.1	RZQ/5	1,2
Pull-up and pull-down mismatch, MMPuPd		VOMdc=0.8*VDDQ	-10		10	%	1,2,3,4
DQ-DQ mismatch within byte (pull-up), MM_PuDd		VOMdc=0.8*VDDQ			10	%	1,2,4
DQ-DQ mismatch within byte (pull-down), MM_PdDu		VOMdc=0.8*VDDQ			10	%	1,2,4

Note 1: This tolerance limit is specified after calibration under stable voltage and temperature. If temperature or voltage changes after calibration, the behavior of the tolerance limit should refer to the subsequent voltage and temperature sensitivity section (TBD).

Note 2: It is recommended to calibrate the output driver impedance for pull-up/pull-down at 0.8*VDDQ. Other calibration schemes may also be used to meet the linearity requirement, such as calibration at 0.5*VDDQ and 0.95*VDDQ.

Note 3: Measurement definition for pull-up and pull-down impedance mismatch (MMPuPd): Measure RONPu and RONPD independently at 0.8*VDD; Ronnom is the nominal Ron value.

$$\mathrm{NMPuPd} = \frac{\mathrm{PONPu} - \mathrm{RONPd}}{\mathrm{RONNOM}} * 100$$

Note 4: Ratio of RON deviation range to nominal RON value in a given component, including DQS_t and DQS_c.

$$\mathrm{NMPuPd} = \frac{\mathrm{RONPuMax} - \mathrm{RONPuMin}}{\mathrm{RONNOM}} * 100$$

$$\mathrm{NMPuPd} = \frac{\mathrm{PONPdMax} - \mathrm{RONPdMin}}{\mathrm{RONNOM}} * 100$$

Note 5: For ×16 devices, this parameter is specified for upper byte and lower byte.

5.2 DC electrical characteristics of output driver for loopback signals LBDQS, LBDQ

DDR5 loopback driver supports 34 ohm impedance. The functional schematic of the output buffer is shown in Figure 5-2. The separate pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

With RONPd off:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$

With RONPu off:

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$

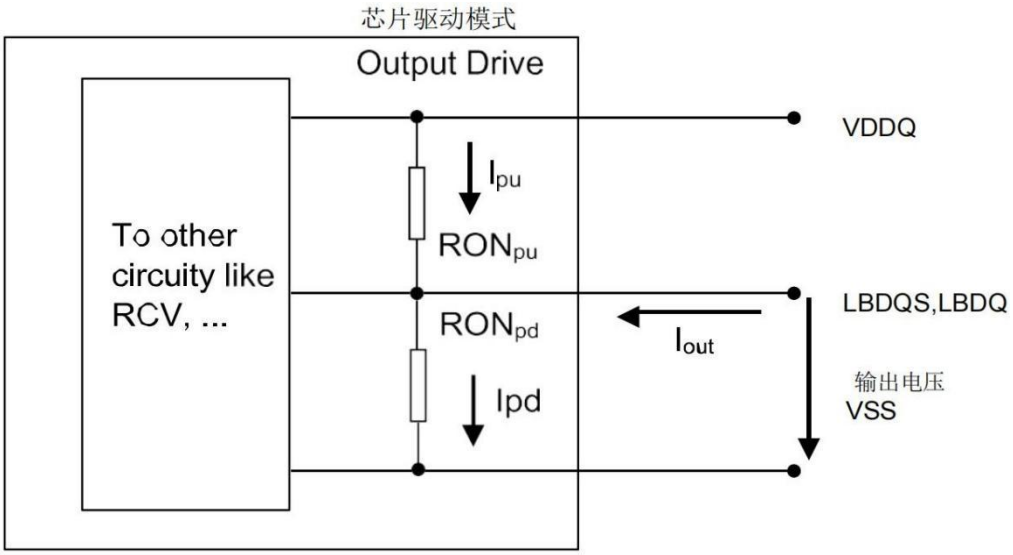


Figure 5-2 Loopback Signal Output Driver

Table 5-2 Output Driver DC Electrical Characteristics

Assuming RZQ = 240 ohms over the entire operating temperature range; after proper ZQ calibration

RONNOM	Resistor	Output Voltage	Min	Nominal	Max	Unit	Note
34Ω	RON34Pd	DC voltage = 0.5*VDDQ	0.8	1.0	1.1	RZQ/7	1,2
		VOMdc=0.8*V_{DDQ}	0.9	1.0	1.1	RZQ/7	1,2
		VOHdc= 0.95*V_{DDQ}	0.9	1.0	1.25	RZQ/7	1,2
	RON34Pu	VOLdc=0.5*V_{DDQ}	0.9	1.0	1.25	RZQ/7	1,2
		VOMdc=0.8*V_{DDQ}	0.9	1.0	1.1	RZQ/7	1,2
		VOHdc=0.95*V_{DDQ}	0.8	1.0	1.1	RZQ/7	1,2
Pull-up and pull-down mismatch, MMPuPd		VOMdc=0.8*V_{DDQ}	-10		10	%	1,2,3,4
Intra-byte DQ-DQ mismatch variation (pull-up), MMPuPd		VOMdc=0.8*V_{DDQ}			10	%	1,2,4
DQ-DQ mismatch (within-byte variation, pull-up), MMPddd		VOMdc=0.8*V_{DDQ}			10	%	1,2,4

Note 1: These tolerance limits are specified after calibration under stable voltage and temperature. If temperature or voltage changes after calibration, the behavior of the tolerance limits is described in a subsequent section on voltage and temperature sensitivity (TBD);
Note 2: Pull-up and pull-down output driver impedance is recommended to be calibrated at 0.8×VDDQ. Other calibration schemes may also be used to achieve the linearity specifications above, e.g., calibration at 0.5×VDDQ and 0.95×VDDQ;
Note 3: Measurement definition of pull-up and pull-down impedance mismatch, MMPuPd: independent measurement of RONPu and RONPd at 0.8×VDDQ; RONNOM is the nominal RON value.

$$NMPuPd = \frac{PONPu - RONPd}{RONNOM} * 100$$

RONNOM	Resistor	Output Voltage	Min	Nominal	Max	Unit	Note
Note 4: Ratio of the deviation range of RON from RON(NOM) within a given device, including LBDQS and LBDQ. $NMPuPd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$ $NMPuPd = \frac{PONPdMax - RONPdMin}{RONNOM} * 100$							

5.3 Loopback Output Timing

The relationship between the loopback strobe signal LBDQS and the loopback data signal LBDQ is shown in Figure 5-3.

- tLBQSH describes the high-level width of the single-ended LBDQS clock pulse.
- tLBQSL describes the low-level width of the single-ended LBDQS clock pulse.
- tLBDQSQ describes the latest valid transition point of LBDQ measured from both rising and falling edges of LBDQS
- tLBQH describes the earliest invalid transition of LBDQ measured from the rising and falling edges of LBDQS
- tLBDVW describes the data valid window per device per interface, calculated as (tLBQH - tLBDQSQ) for each interface on a given DRAM

Table 5-3 DDR5-5600 Loopback Output Timing Parameters

Speed		DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Loopback Timing									
Loopback LBDQS Output Low-Level Time	tLBQSL	0.7	-	0.7	-	0.75	-	tCK	1
Loopback LBDQS Output High-Level Time	tLBQSH	0.7	-	0.7	-	0.75	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.5	-	0.5	-	0.5	-	tCK/2	1
Loopback LBDQ Output Hold Time (Relative to LBDQS)	tLBQH	0.5	-	0.5	-	0.5	-	tCK/2	1
Loopback Data Valid Window per Subchannel (tLBQH - tLBDQSQ)	tLBDVW	1.6	2	1.6	2	1.6	2	tCK/2	1
Note 1: Based on loopback 4-way interleave configuration									

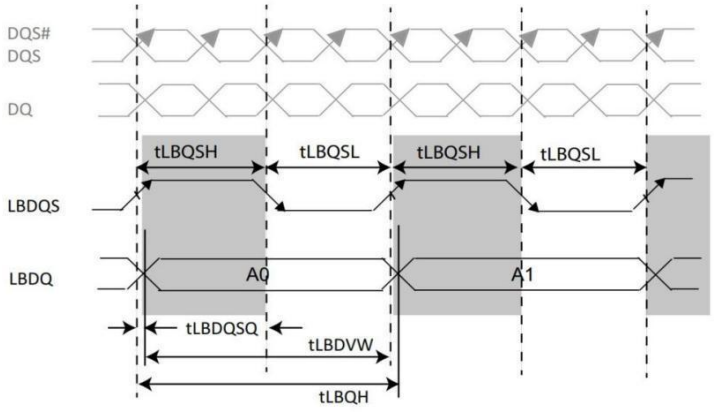


Figure 5-3: Relationship between Loopback Pulse and Data

5.3.1 Connectivity Test (CT) Mode Input Levels

The output buffer functional diagram is shown in Figure 5-4. The output driver impedance RON is defined as: with RONPu turned off:

$$RON_{Pd} = \frac{Vout}{|I\,out|}$$

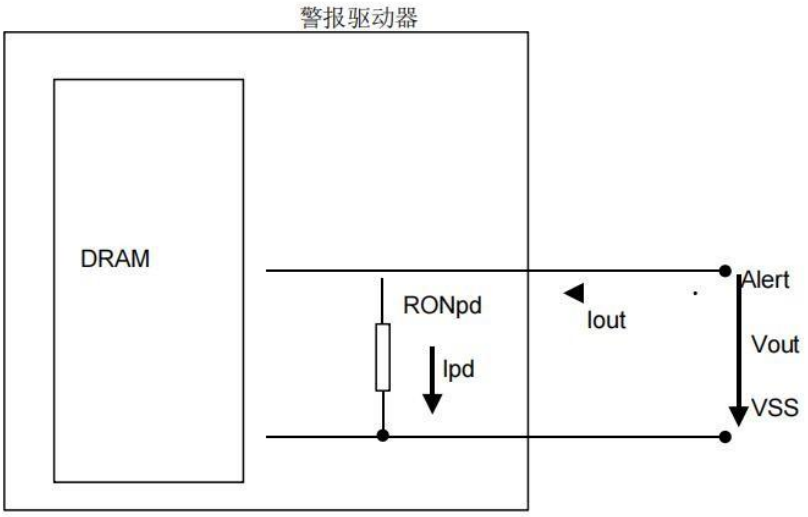


Figure 5-4 Alert Driver

Table 5-4 DDR5-5600 Loopback Output Timing Parameters

Resistance	Vout	Min	Max	Unit	Note
RONPd	VOLdc= 0.1* VDDQ	0.3	1.1	RZQ/7	
	VOMdc= 0.8* VDDQ	0.4	1.1	RZQ/7	
	VOHdc= 0.95* VDDQ	0.4	1.25	RZQ/7	

5.3.2 Connectivity Test (CT) Mode Input Levels

In Connectivity Test (CT) mode, the output driver impedance RON is applied to the test output pins as follows. The separate pull-up/pull-down resistances (RONPu_CT and RONPd_CT) are defined as:

$$RON_{Pu_CT} = \frac{VDDQ - Vout}{|I\,out|}$$

$$RON_{Pd_CU} = \frac{Vout}{|I\,out|}$$

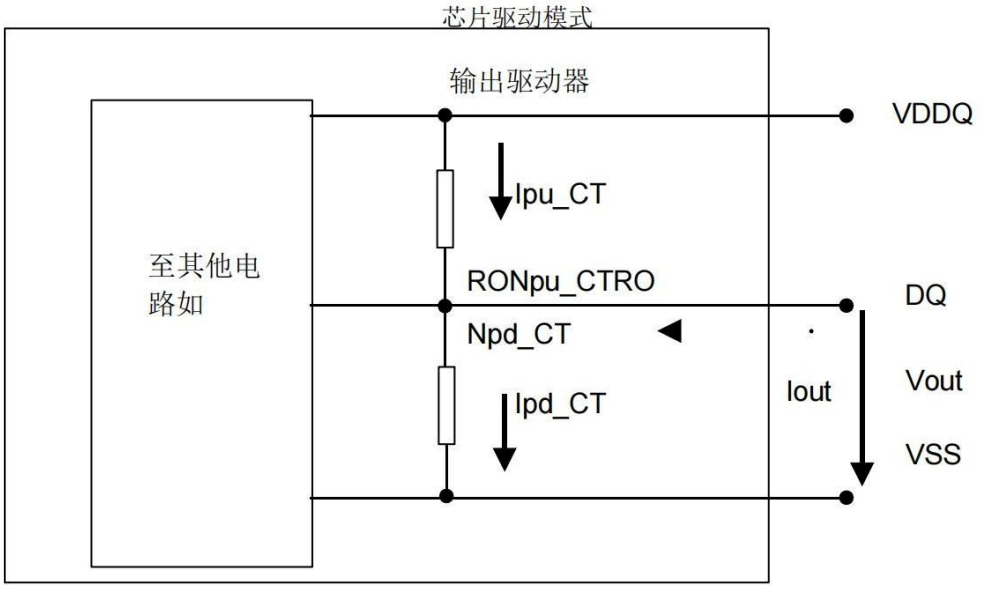


Figure 5-5 Output Driver

Table 5-5 DDR5-5600 Loopback Output Timing Parameters

RONNOM_CT	Resistance	Vout	Max	Unit	Note
34Ω	RONPd_CT	VOBdc=0.2*V_{DDQ}	1.9	RZQ/7	1,2
		VOLdc=0.5*V_{DDQ}	2.0	RZQ/7	1,2
		VOMdc=0.8*V_{DDQ}	2.2	RZQ/7	1,2
		VOHdc=0.95*V_{DDQ}	2.5	RZQ/7	1,2
	RONPu_CT	VOBdc=0.2*V_{DDQ}	1.9	RZQ/7	1,2
		VOLdc=0.5*V_{DDQ}	2.0	RZQ/7	1,2
		VOMdc=0.8*V_{DDQ}	2.2	RZQ/7	1,2
		VOHdc=0.95*V_{DDQ}	2.5	RZQ/7	1,2
Note 1: Connectivity test mode uses an uncalibrated driver, exhibiting full range across PVT. No mismatch is specified between pull-up and pull-down. Note 2: Uncalibrated drive strength tolerance is specified as ±30%.					

5.4 Single-Ended Output Level - VOL/VOH

Table 5-6: Single-Ended Output Levels for DDR5-4800/5600/6400

Symbol	Parameter	DDR5-4800/5600/6400	Unit	Notes
VOH	Output High Level Measurement (for Output SR)	0.75 × Vpp	V	1
VOL	Output Low Level Measurement (for Output SR)	0.25 × Vpp	V	1
Note 1: Vpk-pk refers to the value obtained by subtracting the average low voltage from the average high voltage over a specific number of samples.				

5.5 Single-ended output level - High/low level voltage of loopback signal

Table 5-7 Single-ended Output Levels for Loopback Signal DDR5-4800/5600/6400

Symbol	Parameter	DDR5-4800/5600/6400	Unit	Notes
VOH	Output high level measured value (for output SR)	0.75 × output peak-to-peak voltage	V	1
VOL	Output low measurement level (for output SR)	0.25 × Vpk-pk	V	1
Note 1: Vpk-pk is the average high voltage minus the average low voltage over a specific number of samples.				

5.6 Single-ended Output Slew Rate

When using the timing measurement reference load, the output slew rate for falling and rising edges of a single-ended signal is defined and measured between VOL and VOH.

between VOH; see Table 5-8 and Figure 5-6 for details.

Table 5-8: Single-Ended Output Slew Rate for DDR5-4800/5600/6400

Description	Measured		Definition Basis
	From	To	
Single-Ended Output Rising Edge Slew Rate	VOL	VOH	[VOH-VOL] / delta TRse
Single-Ended Output Falling Edge Slew Rate	VOH	VOL	[VOH-VOL] / delta TFse
Note 1: Output slew rates are verified by design and characterization and may not be subject to production test.			

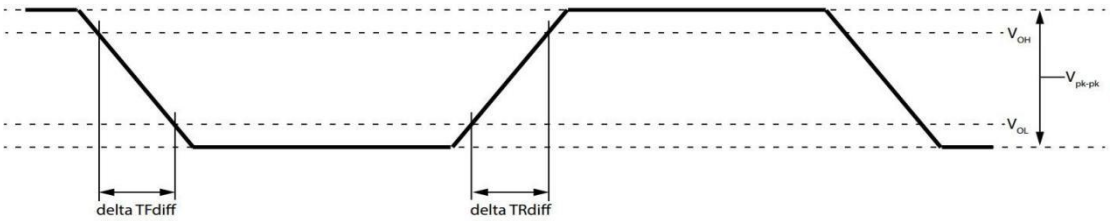


Figure 5-6 Single-Ended Output Slew Rate Definition

Table 5-9 Single-Ended Output Slew Rate for DDR5-5600

Speed		DDR5-5600		Unit	Notes
Parameter	Symbol	Min	Max		
Single-ended Output Slew Rate	SRQse	12	24	V/ns	

5.7 Differential Output Voltage

Table 5-10 DDR5-4800/5600/6400 Differential Output Slew Rate

Symbol	Parameter	DDR5-4800/5600/6400	Unit	Notes
VOHdiff	Differential Output High Level Measurement Value (for output SR)	0.75 × Vdiffpk-pk	V	1
VOLdiff	Differential Output Low Level Measurement Value (for output SR)	0.25 × Vdiffpk-pk	V	1
Note 1: Vdiffpk-pk is the average high voltage minus average low voltage in a TBD sample.				

5.8 Differential output slew rate

When timing measurements are performed using the reference load, the rising and falling edge output slew rates for differential signals are defined and measured between VOLdiff and VOHdiff, as detailed in Table 5-11 and Figure 5-7.

Table 5-11 Differential Output Slew Rate Definition

Description	Measured		Definition Basis
	From	To	
Differential Output Rising Edge Slew Rate	VOLdiff	VOHdiff	[VOHdiff-VOLdiff] / delta TRdiff
Differential Output Falling Edge Slew Rate	VOHdiff	VOLdiff	[VOHdiff-VOLdiff] / delta TFse
Note 1: Output slew rate is verified by design and characterization analysis; no production test is required.			

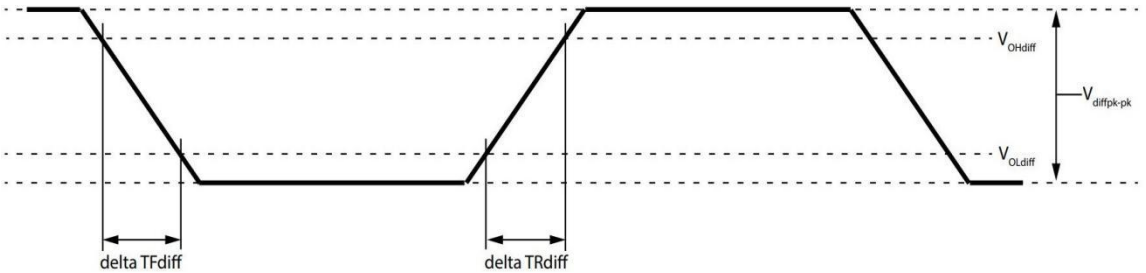


Figure 5-7 Differential Output Slew Rate Definition

Table 5-12 Differential Output Slew Rate for DDR5-4800/5600/6400

Speed		DDR5-4800/5600/6400		Unit	Note
Parameter	Symbol	Min	Max		
Differential output slew rate	SRQdiff	16/24/24	48/48/48	V/ns	

5.9 Tx DQS jitter

The specified random jitter (Rj) is random jitter with a Gaussian distribution. The specified deterministic jitter (Dj) is bounded jitter.

The output jitter of DDR5 devices must not exceed the maximum values specified in Table 5-13.

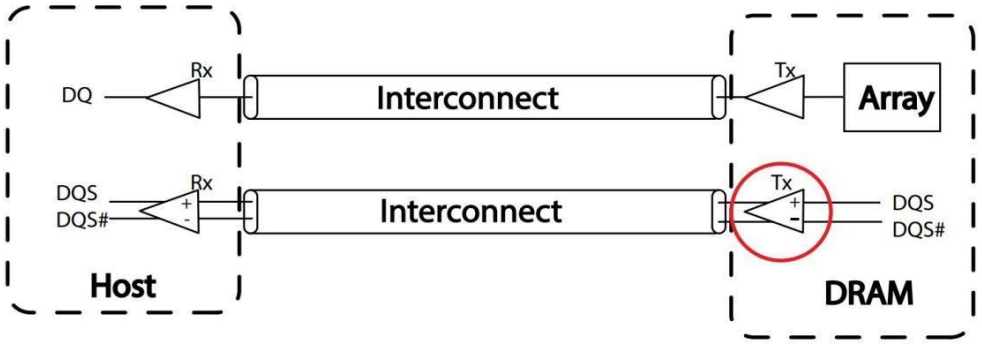


Figure 5-8 Tx DQS Jitter Interconnect

Table 5-13 Tx DQS Jitter Parameters for DDR5-4800/5600/6400

Dj = deterministic jitter; Rj = random jitter; DCD = duty cycle distortion; BUJ = bounded uncorrelated jitter; pp = peak-to-peak]

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Rj (1-UI) RMS (no BUJ)	tTx_DQS_1UI_Rj_noBUJ	-	tCK_1UI_Rj_noBUJ+0.002	-	tCK_1UI_Rj_noBUJ+0.002 BUJ+0.002	-	TBD	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj (pp) 1-UI jitter value (without BUJ)	tTx_DQS_1UI_Dj_withBUJ with BUJ	-	0.150	-	0.130	-	TBD	UI	1,2,3,5,6, 7,8,9,10, 11
Rj RMS value for N-UI jitter value, not including BUJ, where 1<N<4	tTx_DQS_NUI_Rj_oBUJ	-	tCK_NUI_Rj_NoBUJ+0.002	-	tCK_NUI_Rj_NoBUJ BUJ+0.002	-	TBD	UI (RMS)	1,2,3,5,6, 7,8,9,10, 11,12
Dj pp N-UI jitter without BUJ, where 1<N<4 1<N<4	tTx_DQS_NUI_Dj_oBUJ	-	0.150	-	0.130	-	TBD	UI	1,2,3,5,6, 7,8,9,10, 11

Note 1: On-chip noise similar to that generated when all transmitter and receiver channels are switching must be simulated. When there is no socket in the transmitter measurement setup, even if all transmitter channels transmit test patterns, the impact of crosstalk is typically insignificant or can be estimated within acceptable error. If a socket is present (e.g., the DUT is a DRAM component), the impact of crosstalk may be significant. To minimize the impact of crosstalk on measurement results, selected groups of channels adjacent to the channel under test can be turned off (transmitting DC signals), while the remaining transmitter channels send signal patterns to corresponding receivers, thereby exciting a realistic on-chip noise characteristic from device switching. Note: When one of the Dj and Rj specifications meets the requirement but the other fails, signal analysis should be performed to determine link feasibility.

Note 2: On-chip noise similar to that generated when all transmitter and receiver channels are switching must be simulated. When no socket is connected in the transmitter measurement setup, even if all transmitter channels send test patterns, the contribution of BUJ is usually insignificant or within tolerable error. If a socket is present (e.g., the DUT is a DRAM component), the contribution of BUJ may be significant. To minimize the impact of BUJ on measurement results, a group of selected channels near the channel under test can be turned off (sending DC signals), while the remaining transmitter channels send signal patterns to their corresponding receivers, thereby exciting the

real on-chip noise characteristics generated by device switching.

5.10 Tx DQ jitter

5.10.1 Overview

The specified random jitter (Rj) is random jitter with a Gaussian distribution. The specified deterministic jitter (Dj) is bounded jitter.

The output jitter of DDR5 devices must not exceed the maximum values specified in Table 5-14.

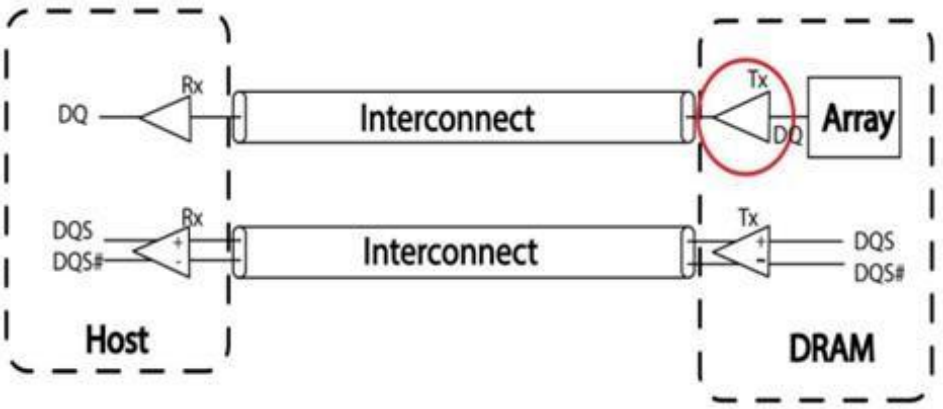


Figure 5-9 Tx DQ Jitter Interconnect

Table 5-14 Tx DQ Jitter Parameters for DDR5-5600

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
RMS value of Rj (1-UI) without BUJ jitter	tTx_DQ_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ+0.002 02	-	tCK_1UI_Rj_ NoBUJ+0.0 02	-	TBD	UI (RMS)	1,3,4,5,7,8,9, 10,11,12,13, 14
Peak-to-peak Dj (1-UI) without BUJ jitter	tTx_DQ_1UI_Dj_NoBUJ	-	0.150	-	0.130	-	TBD	UI	3,5,7,8,9,10, 11,12,13,
RMS value of Rj for N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_ NoBUJ+0.002	-	tCK_NUI_Rj_ NoBUJ+0.002	-	TBD	UI (RMS)	3,5,7,8,9,10, 11,12,13,14,

DJ pp jitter for N-UI without BUJ, where 1<N<4	tTx_DQ_NUI_DJ_noBUJ	-	0.150	-	0.130	-	TBD	UI	3,6,7,8,9,10, 11, 12,13
Delay of any data path relative to clock path	tTx_DQS2DQ		0.100		0.100		TBD	UI	3,5,6,7,9,10, 11,12,13

Note 1: On-chip noise similar to that generated when all transmitter and receiver channels are switching must be simulated. When there is no socket in the transmitter measurement setup, even if all transmitter channels transmit test patterns, the impact of crosstalk is typically insignificant or can be estimated within acceptable error. If a socket is present (e.g., the DUT is a DRAM component), the impact of crosstalk may be significant. To minimize the impact of crosstalk on measurement results, selected groups of channels adjacent to the channel under test can be turned off (transmitting DC signals), while the remaining transmitter channels send signal patterns to corresponding receivers, thereby exciting a realistic on-chip noise characteristic from device switching. Note: When one of the Dj and Rj specifications meets the requirement but the other fails, signal analysis should be performed to determine link feasibility.
Note 2: On-chip noise generated when all transmitter and receiver channels are switching must be simulated. When there is no socket in the transmitter measurement setup, even if all transmitter channels transmit test sequences, the contribution of BUJ is typically insignificant or can be estimated within acceptable error. When a socket is present (e.g., the DUT is a DRAM device), the contribution of BUJ may be significant. To minimize the impact of BUJ on measurement results, selected groups of channels adjacent to the channel under test can be turned off (transmitting DC signals), while the remaining transmitter channels send signal sequences to corresponding receivers, thereby exciting a realistic on-chip noise characteristic from device switching. Note: When one of the DJ and RJ specifications meets the requirement but the other fails, signal analysis should be performed to determine link feasibility.
Note 3: The verification method for these parameters will be covered in a future ballot.
Note 4: RJ rms value is 1-UI jitter (excluding BUJ), but on-chip noise similar to system noise exists. This extraction must be performed after software DCD correction. Note 5: Any data channel delay relative to the clock channel, measured at the transmitter output.
Note 6: Vref noise level and DQ jitter should be adjusted to
minimize DCD. Note 7: Minimum BER requirements are
detailed in Section 7.2.
Note 8: Definitions of UI, NUI, and jitter are detailed in Section 7.3.
Note 9: Before running this test, the duty cycle of the DQ pins must be adjusted to as close to 50% as possible using global and per-pin duty cycle adjustment features.
Note 10: The mode registers for duty cycle adjuster are MR43 and MR44. Additionally, per-pin DCA mode registers for DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$; per-pin DCA mode registers for DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
Note 11: Spread spectrum clocking (SSC) must be disabled when performing this test.
Note 12: These parameters are tested using the continuous clock mode output from the DRAM device, without sending consecutive MRR commands. Set MR25 OP[3] to "1" to enable this feature.
Note 13: Tested on CTC2 card only.
Note 14: The maximum values of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ are up to 6 mUI RMS.

5.11 Tx DQ Stress Eye Diagram

At a BER of 1e-16 and 99.5% confidence level, the height and width of the Tx DQ stress eye diagram must meet the minimum specification requirements. The Tx DQ stress eye diagram shows the DQS-to-DQ timing skew in both eye width and eye height directions. To accommodate different host receiver (Rx) designs, the host shall adjust the DQS preamble position accordingly by reading the DQS offset timing mode register setting (MR40 OP[3:0]).

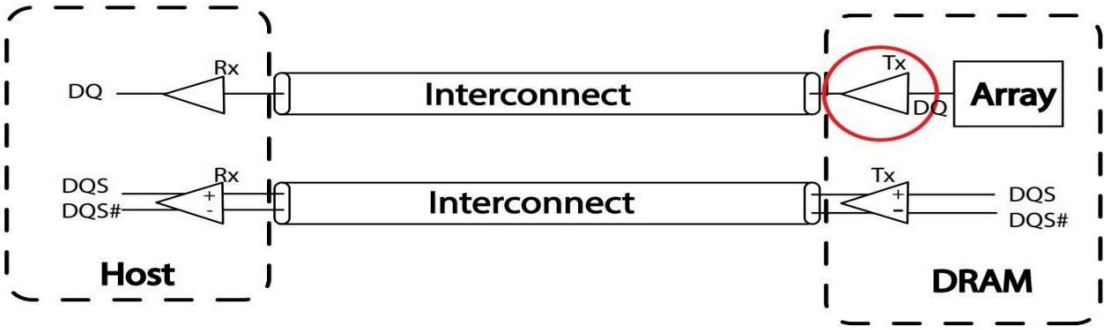


Figure 5-10 DDR5 Memory Interconnection Example

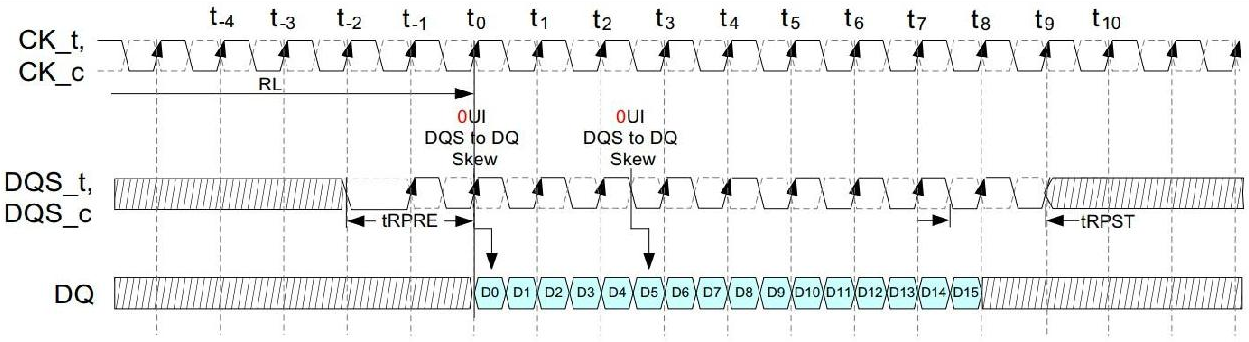
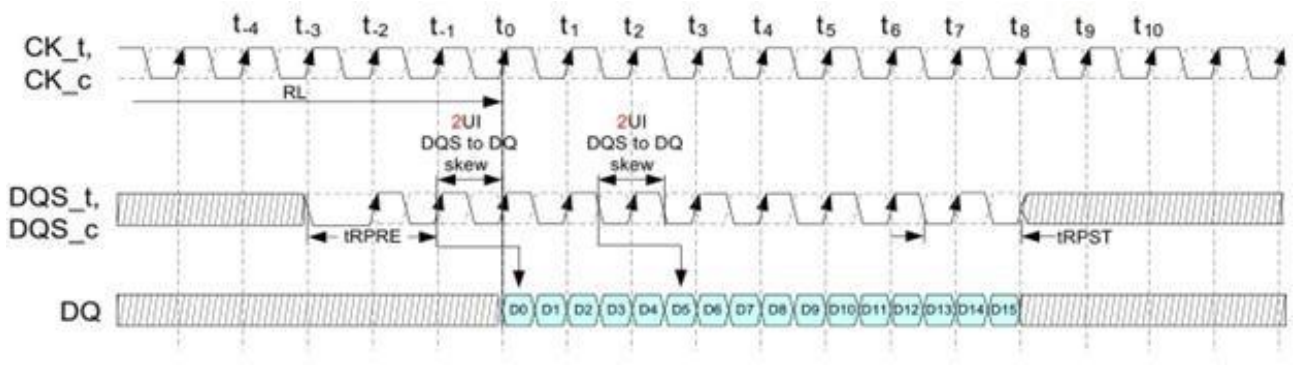


Figure 5-11 Read Burst Example for DQx Pins, Showing Timing Relationship of Bit 0 and Bit 5 Relative to DQS Edge (0 UI



Offset)

Figure 5-12 Read Burst Example

For DQx pins, when the read DQS offset timing is set to 1 clock cycle (2 UI), shows the state of bit 0 and bit 5 relative to the DQS edges.

5.11.1 Tx DQ Stress Eye Diagram Parameters

Table 5-15 Tx DQ Stress Eye Parameters for DDR5-4800/5600/6400

[EH = Eye Height, EW = Eye Width; BER = Bit Error Rate, SES = Stress Eye Shift]

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Transmitter specified offset, DQ and DQS have 1UI offset	TxEH_DQ_SES_1UI	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,6, 7,8,9,10
Transmitter-specified eye width for DQ with Transmitter-specified eye width for DQ with 1 UI offset between DQ and DQS	TxEW_DQ_SES_1UI	-	0.72	-	0.74	-	TBD	UI	1,2,3,4,6, 7,8,9,10
Transmitter-specified eye height for DQ with 2 UI offset between DQ and DQS	TxEH_DQ_SES_2UI	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,6, 7,8,9,10
Transmitter-specified Eye Height, DQ with Tx specified eye width, with 2UI offset between DQ and DQS	TxEW_DQ_SES_2UI	-	0.72	-	0.74	-	TBD	UI	1,2,3,4,6, 7,8,9,10
Tx specified eye height, with 3UI offset between DQ and DQS	TxEH_DQ_SES_3UI	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,6, 7,8,9,10
Transmitter-specified Eye Height, DQ with Tx specified eye width, with 3UI offset between DQ and	TxEW_DQ_SES_3UI	-	0.72	-	0.74	-	TBD	UI	1,2,3,4,6, 7,8,9,10

DQS									

Transmitter-specified Eye Height, DQ with Transmitter-specified Eye Height, DQ with DQS offset of 4UI	TxEH_DQ_SES_4UI	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,5, 6,7,8,9,10
Transmitter-specified Eye Height, DQ with DQS offset of 4UI	TxEW_DQ_SES_4UI	-	TBD	-	0.74	-	TBD	UI	1,2,3,4,5, 6,7,8,9,10
Transmitter eye height, DQ to DQS with 5UI offset	TxEH_DQ_SES_5UI	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,5, 6,7,8,9,10
Transmitter eye width, DQ to DQS with 5UI offset	TxEW_DQ_SES_5UI	-	TBD	-	TBD	-	TBD	UI	1,2,3,4,5, 6,7,8,9,10

Note 1: Minimum BER of E-9 per pin with 99.5% confidence level; Note 2: Per DDR5 minimum bit error rate (BER) requirement; Note 3: The verification methodology for these parameters will be covered in future ballots.
Note 4: Mismatch is defined as the mismatch between DQS and DQ, measured in UI increments.
Note 5: The number of accumulated UI depends on the link speed. High-speed links may specify higher accumulated UI values; for low-speed links, N=4 or 5 UI may not be applicable. Note 6: Before running this test, the duty cycle of the DQ pins must be adjusted as close to 50% as possible using global and per-pin duty cycle adjuster (DCA) functions.
Note 7: The mode registers for the duty cycle adjuster are MR43 and MR44. In addition, the per-pin DCC mode registers for DQS are MR103-MR110, the independent DCA mode registers for DQLx pins are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$; the independent DCA mode registers for DQUy pins are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
Note 8: Spread spectrum clocking (SSC) must be disabled during this test.
Note 9: These parameters are tested using a continuous PRBS8 LFSR training pattern, which is sent through all DQ channels of the DRAM device without requiring continuous MRR commands. Bit OP[3] of MR25 must be set to '1' to enable this function. Tested on CTC2 card only.

6. Speed Parameter

6.1 DDR5 Speed Parameters and Operation

Table 6-1 DDR5-4800 Speed Parameters and Operation

Speed Parameter					DDR5-4800		Unit	Notes
CL-nRCD-nRP					40-39-39			
Parameter				Symbol	Min	Max		
Read command to first data				tAA	16.000	22.222	ns	12
Row address to column address delay				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Active to Precharge command period				tRAS	32.000	5 * tREFI1 (standard) 9 *tREFI2(FGR)	ns	7
ACT to ACT or REF command period				tRC(tRAS+tRP)	48.000	-	ns	7,8
CAS write latency				CWL	CWL=CL-2		nCK	
Speed Parameter	tAAmin (ns)[5]	tRCDmin, tRPmin (ns)5	Read CL12	Supported Minimum Frequency Range				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(avg)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(avg)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(avg)	Reserved		ns	
3600C	17.777	17.777	32	tCK(avg)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(avg)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(avg)	Reserved		ns	
4000C	18.000	17.500	36	tCK(avg)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(avg)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(avg)	Reserved		ns	
4400C	18.181	17.727	40	tCK(avg)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(avg)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(avg)	Reserved		ns	
4800C	17.500	17.500	42	tCK(avg)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(avg)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(avg)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(avg)	Reserved		ns	
Supported CL					22,26,28,30,32,36,40,42		nCK	12

Speed Grade					DDR5-5600		Unit	Note
CL-nRCD-nRP					46-45-45			
Parameter				Symbol	Min	Max		
Read command to first data latency				tAA	16.000	22.222	ns	12
Read/Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Active to Precharge command period				tRAS	32.000	5 * tREFI1 (standard) 9 *tREFI2(FGR)	ns	7
ACT to ACT or REF command period				tRC(tRAS+tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL	CWL=CL-2		nCK	
Speed Bin	tAAmin (ns)5	tRCDmin tRPmin (ns)5	Read CL12	Supported Minimum Frequency Range				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6.9
3200C	17.500	17.500	28	tCK(avg)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(avg)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(avg)	Reserved		ns	
3600C	17.777	17.777	32	tCK(avg)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(avg)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(avg)	Reserved		ns	
4000C	18.000	17.500	36	tCK(avg)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(avg)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(avg)	Reserved		ns	
4400C	18.181	17.727	40	tCK(avg)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(avg)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(avg)	Reserved		ns	
4800C	17.500	17.500	42	tCK(avg)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(avg)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(avg)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(avg)	Reserved		ns	
5200C	17.692	17.692	46	tCK(avg)	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(avg)	0.384	<0.416	ns	
5200AN	14.615	14.615	38	tCK(avg)	Reserved		ns	
5600C	17.857	17.500	50	tCK(avg)	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(avg)	0.357	<0.384	ns	
5600B	16.428	16.071	46	tCK(avg)	0.357	<0.384	ns	
5600AN	14.285	14.285	40	tCK(avg)	Reserved		ns	
Supported CL					22,26,28,30,32,36,40,42,46,50		nCK	12

Table 6-3 DDR5-6400 Speed Bins and Operations

Speed Bin					DDR5-6400		Unit	Notes
CL-nRCD-nRP					52-52-52			
Parameter				Symbol	Min	Max		
Read command to first data				tAA	16.000	22.222	ns	12
Read/Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
ACT to PRE command period				tRAS	32.000	5 *tREFI1(Norm) 9 *tREFI2r(FGR)	ns	7
ACT to ACT or REF command period				tRC(tRAS+tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL	CWL=CL-2		nCK	
Speed Bin	tAAmin (ns)[5]	tRCDmin + tRPmin (ns)[5]	Read CL12	Supported Downclocking Range				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	Reserved		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	Reserved		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	Reserved		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	Reserved		ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(AVG)	Reserved		ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	ns	
5200AN	14.615	14.615	38	tCK(AVG)	Reserved		ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	ns	
5600AN	14.285	14.285	40	tCK(AVG)	Reserved		ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	ns	
			42	tCK(AVG)	Reserved		ns	

6000AN	14.000	14.000						
6400C	17.500	17.5000	56	tCK(AVG)	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	ns	
6400AN	14.375	14.375	46	tCK(AVG)	Reserved		ns	
Supported CL					22,26,28,30,32,36,40,42,46,50,52,54,56		nCK	12

DDR5 Speed Binning Table Notes:

1. Minimum timing parameters are defined according to the rules in the "Rounding Definitions and Algorithms" section.
2. All timing parameter conversions from ns values to nCK values shall follow the rounding algorithm. The conversion from tAA to CL shall follow the specific combinations listed in the speed binning table.
3. The CL setting together with the CWL setting determines tCK(avg)min and tCK(avg)max requirements. When selecting tCK(avg), both the CL setting and the CWL setting requirements must be satisfied.
4. The "Reserved" setting is prohibited; the user must program other values.
5. This column displays the planned replacement and supported native speed bin timings for downclocking. This column does not necessarily show the minimum speed bin timings allowed and supported for downclocking because, per the rounding algorithm, timings may be faster depending on the combination of the specific speed bin and the downclocked frequency.
6. When the DRAM is operating at a data rate lower than 4800 MT/s, DDR5-4800 AC timing parameters apply. This rule applies not only to the timing parameters in the speed bin table.
7. The parameter applies over the range from tCK(avg)min to tCK(avg)max.
8. tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithm, nRC(min)
   shall always be greater than or equal to nRAS(min) + nRP(min).
9. tCK(avg)max is defined as 1.010 ns (1980 MT/s data rate) to meet the 1% SSC downward spread requirement at 2000 MT/s data rate per JESD79-4.
10. Each speed bin lists the timing requirements that a specific DRAM must support to comply with the JEDEC standard. The JEDEC standard does not require supporting all speed bins within a given speed range; it requires only meeting the parameters of at least one listed speed bin.
11. Any speed bin supports functional operation at lower frequencies (as shown in the table). Such operation does not require production test qualification, but must be design/characterization verified.
12. The CL algorithm can be used to determine the valid CAS latencies listed in the speed bin table. This algorithm calculates the supported CAS latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Based on the computed tCK(AVG)min value and the rate-range target timings, the CL algorithm computes the valid CAS latency using a rounding algorithm. Since the DDR5 SDRAM specification supports only even CAS latencies, odd
13. CAS latencies are rounded up to the nearest even value. The 1980–2100 MT/s data rate always uses CL22. If

tAA(corrected) or tRCDtRP(corrected) is violated, the CL algorithm will use a slower tAA(target) and tRCDtRP(target) combination to

14. return a slower valid CAS latency. A DDR5 SDRAM can support up to four valid CAS latencies at a given frequency: CL(AN), CL(B), CL(BN), and CL(C). The corrected tAA(corrected) and tRCDtRP(corrected) are calculated by multiplying tAA(min), tRCD(min), and tRP(min) by the rounding algorithm correction factor. The correct setting for CL should be determined by the memory controller, and can be achieved using the speed bin table, the CL algorithm, or other methods. For more information, refer to the "Rounding Definitions and Algorithm" chapter. When CRC is enabled, the CL value is incremented based on the Read CRC Latency Accumulator. There is no Write CRC Latency Accumulator when CRC is enabled, so CWL is still calculated based on the CL value when CRC is disabled.

6.2 tREFI and tRFC Parameters

Table 6-4 tREFI and tRFC Parameters

Command	Refresh Mode	Symbol & Range		Expression	Value	Unit	Notes
REFab	Normal Mode	tREFI1	0°C<= TCASE<= 85°C	rREFI	3.9	us.	
			85°C< TCASE<= 95°C	rREFI/2	1.95	us.	
REFab	High-Precision	tREFI2	0°C<= TCASE<= 85°C	rREFI/2	1.95	us.	
			85°C< TCASE<= 95°C	rREFI/4	0.975	us.	
REFsb	High-Precision	tREFIsb	0°C<= TCASE<= 85°C	tREFI/(2*n)	1.95/n	us.	1
			85°C< TCASE<= 95°C	tREFI/(4*n)	0.975/n	us.	1

Notes:

1. n is the number of banks in a bank group (e.g., 8Gb: n=2; 16Gb: n=4)

7. IDD and IDDQ Specifications and Test Conditions

7.1 IDD, IPP, and IDDQ Measurement Conditions

This chapter defines the measurement conditions for IDD, IPP, and IDDQ, including test loads and test modes. Figure 7-1 shows the test setup and test loads for IDD, IPP, and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7,
  IDD8, IDDQ8, IPP8, and IDD9, IDDQ9, IPP9) are all measured as time-averaged currents.
- All measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test connected together. Any IDDQ or IPP currents are not included in the IDD current.
- IDDQ current is measured as a time-averaged current with all VDDQ pads of the DDR5 SDRAM under test connected. IDDQ current does not include any IDD or IPP current.
- IPP current is measured as a time-averaged current after connecting all VPP ball of the DDR5 SDRAM under test. Any IDD or IDDQ current is not counted in the IPP current value.

Note: IDDQ values cannot be directly used to calculate I/O power consumption of the DDR5 SDRAM. They can be used to support the correlation between simulated I/O power consumption and actual I/O power consumption, as shown in Figure 7-2.

For IDD, IPP, and IDDQ measurements, the following definitions apply:

- "0" and "low level" are defined as VIN <= VILAC(max).
- "1" and "high level" are defined as input voltage >= VIHAC(min).
- "mid-level" is defined as input voltage VIN equal to VREF, where VREF = 0.75 × VDDQ.
- The basic IDD, IPP, and IDDQ measurement conditions are detailed in Table 7-1.
- Detailed IDD, IPP, and IDDQ measurement loop patterns are described in Sections 7.2 through 7.11.
- IDD measurements must be performed after the DDR5 SDRAM has completed proper initialization and training. This includes, but is not limited to, setting
  - Disable TDQS_t in MR5;
  - Disable CRC in MR5;
  - Disable DM in MR5;
  - Enable 1N mode in MR2 and set CS assertion duration (MR2: OP[4]) to 1, unless otherwise specified in the condition definitions of the IDD, IDDQ, and IPP test patterns;

- Note: The IDD, IDDQ, and IPP measurement loop patterns must be executed at least once before actual measurement begins, with the exception of the IDD9 pattern, which can be measured at any time after the DRAM enters MBIST mode;
- TCASE is defined as 0°C to 95°C, unless otherwise specified in the specific condition definitions of Table 7-1;
- All timing parameters for IDD, IDDQ, and IPP measurements must reference the timing parameters defined in the specification to calculate the required nCK.
  value.

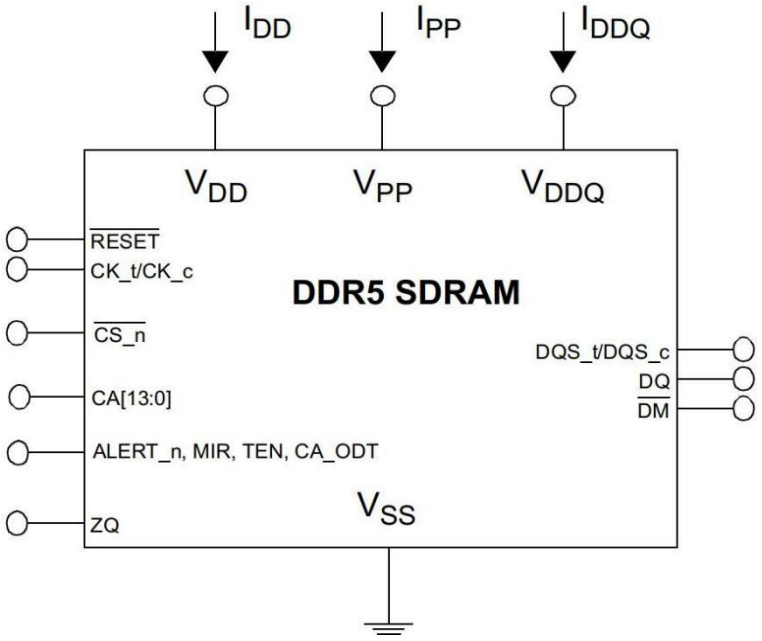


Figure 7-1 Measurement Setup and Test Load for IDD, IPP, and IDDQ Measurements

Note: The output test load conditions at the DIMM level may differ from those shown above.

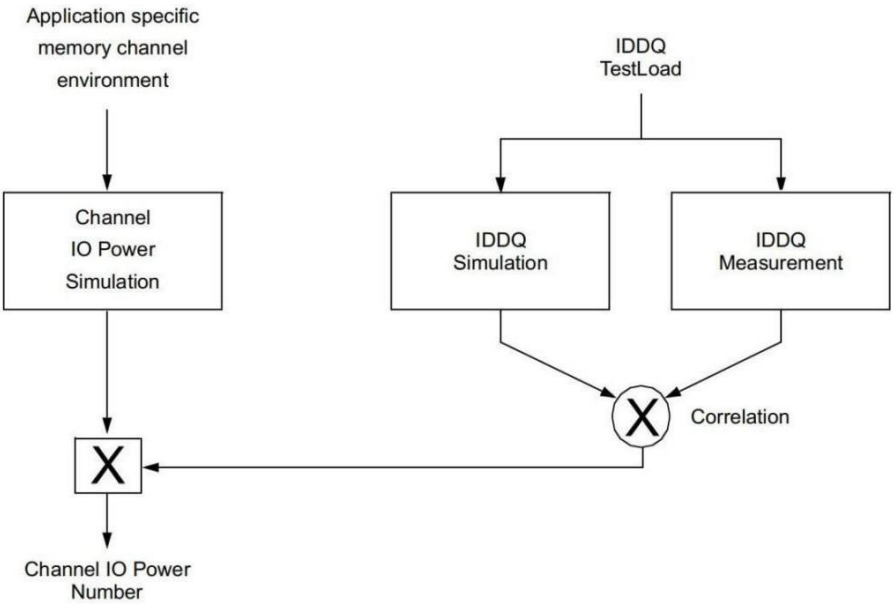


Figure 7-2 Correlation Between Analog Channel Input/Output Power and Actual Channel Input/Output Power Supported by IDDQ Measurement

Table 7-1 Basic IDD, IPP, and IDDQ Measurement Conditions

Symbol	Description
IDD0	Single bank operation, active precharge current, external clock: on; tCK, nRC, nRAS, nRP, nRRD: see Section 13.3 for timing parameters of different speed grades; BL:16; CS_n: remains High between ACT and PRE; CA input: partially toggling according to Table 7-2; Data input/output: VDDQ; DM_n: stable at 1; Memory bank activity: cycling operation, only one bank active at a time: 0,0,1,1,2,2,... (see Table 7-2); Output buffer and termination resistor: enabled in Mode Register 2; Mode details: see Table 7-2
IDDQ0	Single bank operation active precharge IDDQ0 current Same conditions as IDD0, but measuring IDDQ0 current instead of IDD0 current
IPP0	Single bank active precharge IPP0 current Same conditions as IDD0, but measure IPP0 current instead of IDD0 current
IDD0F	Four bank group active precharge current operating state; external clock: on; tCK, nRC, nRAS, nRP, nRRD: see Section 13.3 "Timing Parameters by Speed Grade"; BL:161; CS_n: high between ACT and PRE; CA inputs: partially switching according to Table 7-3; data I/O: VDDQ; DM_n: steady at 1; Bank activity: cycling, activating four banks at a time (see Table 7- 3); output buffer and RTT: enabled in mode register 2; Mode details: see Table 7-3
IDDQ0F	IDDQ current in four-bank simultaneous precharge state Same conditions as IDD0F, but measuring IDDQ current instead of IDD current
IPP0F	Active precharge IPP current in four-bank active state Same conditions as IDD0F, but measuring IPP current instead of IDD current
IDD2N	Precharge standby current External clock: ON; tCK: Refer to Section 13.3 for timing parameters by speed grade; CS_n: Stable at 1; CA inputs: Partially toggling according to Table 7-4; Data I/O: VDDQ; DM_n: Stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in Mode Register 2; Mode details: Refer to Table 7-4
IDDQ2N	Precharge standby IDDQ current Same conditions as IDD2N, but measures IDDQ current instead of IDD current
IPP2N	Precharge standby IPP current Same conditions as IDD2N, but measures IPP current instead of IDD current

Symbol	Description
IDD2NT	Precharge standby non-target command current External clock: on; tCK: see Section 9.3 for timing parameters by speed grade; BL: 16; CS_n: held high between write commands; CS_n, CA inputs: toggling partially according to Table 7-5; data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode register 2; mode details: see Table 7-5
IDDQ2NT (optional)	Precharge Standby Non-Target Command IDDQ Current Same conditions as IDD2NT, but measuring IDDQ current instead of IDD current
IPP2NT (optional)	Precharge Standby Non-Target Command IPP Current Same conditions as IDD2NT, but measuring IPP current instead of IDD current
IDD2P	Precharge power-down Device is in Precharge Power-Down mode; External clock: On; tCK: see Section 9.3 for speed grade timing parameters; CS_n: stable at 1 after Power-Down Entry command; CA input: stable at 1; CA11 = High during PDE command; Data input/output: VDDQ; DM_n: Stable at 1; Bank group activity: All bank groups closed; Output buffers and RTT: Enabled in mode register 2;
IDDQ2P	Precharge power-down Same conditions as IDD2P, but measuring IDDQ current instead of IDD current
IPP2P	Precharge power-down Same conditions as IDD2P, but measuring IPP current instead of IDD current
IDD3N	Active standby current: External clock: On; tCK: See Chapter 9.3 Timing Parameters by Speed Grade; CS_n: Stable at 1; CA inputs: Partially toggling per Table 7-4; DQ: VDDQ; DM_n: Stable HIGH; Bank activation: All banks active; Output buffer and RTT: Enabled in Mode Register 2; Mode details: Refer to Table 7-4
IDDQ3N	Active Standby IDDQ Current Same condition as IDD3N, but measuring IDDQ current instead of IDD current
IPP3N	IPP Current Same conditions as IDD3N, but measuring IPP current instead of IDD current.

Symbol	Description
IDD3P	Active Power-Down Current Device is in active power-down mode; External clock: On; tCK: See Section 9.3 for timing parameters by speed grade; CS_n: Stable at 1 after entering power-down state; CA inputs: Stable at 1; CA11 = HIGH during PDE command; Data I/Os: VDDQ level; DM_n: stable at 1; Bank activation: All banks active; Output buffer and RTT: enabled in Mode Register 2;
IDDQ3P	Active power-down IDDQ current Same conditions as IDD3P, but measures IDDQ current instead of IDD current
IPP3P	Active power-down IPP current Same conditions as IDD3P, but measures IPP current instead of IDD current
IDD4R	Burst read current; External clock: on; tCK, nCCD, CL: see Section 9.3 for timing parameters by speed grade; BL:161; CS_n: high during RD operations; CA inputs: partially toggling according to Table 7-6; Data I/O: seamless read data bursts with different data between consecutive bursts (according to Table 7-6); DM_n: static HIGH; Bank activity: all banks active, RD commands cycling through bank groups in order 0,0,1,1,2,2... (see Table 7-6); Output buffers and RTT: enabled in Mode Register 2; Mode details: see Table 7-6
IDD4RC	Read burst current with read CRC: Read CRC enabled. All other conditions are per IDD4R
DDQ4R	Operating burst read IDDQ current Same definition as IDD4R, but measures IDDQ current instead of IDD current
IPP4R	Operating burst read IPP current Same conditions as IDD4R, but measuring IPP current instead of IDD current
IDD4W	Burst write current External clock: On; tCK, nCCD, CL: See Chapter 9.3 for timing parameters by speed grade; BL:161; CS_n: stays high between write operations; CA inputs: partially toggling according to Table 7-7; Data Input/Output: seamless write data burst according to Table 7-7, with different data between consecutive bursts; DM_n: stable at 1; Bank activity: all banks active, WR commands cycled in order 0,0,1,1,2,2... (see Table 7-7); Output buffer and RTT: enabled in Mode Register 2; Mode details: see Table 7-7
IDD4WC	Operating burst write current (when write CRC enabled) Write CRC enabled 3, other conditions: see IDD4W

Symbol	Description
IDDQ4W	Operating burst write IDDQ current Same conditions as IDD4W, but measures IDDQ current instead of IDD current
IPP4W	Operating burst write IPP current Same conditions as IDD4W, but measures IPP current instead of IDD current
IDD5B	Burst refresh current (normal refresh mode) External clock: enabled; tCK, nRFC1: Refer to Chapter 9.3 'Timing Parameters by Speed Grade'; BL:161; CS_n: High during REF; CA inputs: toggling according to Table 7-8; Data I/O: VDDQ; DM_n: steady at 1; Bank activity: REF command every nRFC1 (refer to Table 7-8); Output buffers and RTT enabled in mode registers; Mode details: refer to Table 7-8
IDDQ5B	Burst refresh IDDQ current (normal refresh mode) Same conditions as IDD5B, but measuring IDDQ current instead of IDD current
IPP5B	Burst refresh IPP current (normal refresh mode) Same conditions as IDD5B, but measuring IPP current instead of IDD current
IDD5F	Burst refresh current (fine granularity refresh mode) tRFC = tRFC2, other conditions: see IDD5B
IDDQ5F	Burst refresh IDDQ current (fine granularity refresh mode) Same conditions as IDD5F, but measuring IDDQ current instead of IDD current
IPP5F	Burst refresh IPP current (fine granularity refresh mode) Same conditions as IDD5F, but measuring IPP current instead of IDD current
IDD5C	Burst refresh current (same bank refresh mode) External clock: on; tCK, nRFCsb: see timing parameters for different speed grades in Chapter 9.3; BL: 16; CS_n: high during REF; CA inputs: partial toggling per Table 7-9; Data input/output: VDDQ; DM_n: stable at 1; Bank activity: REF command executed every nRFCsb (see Table 7-9); output buffer and RTT: enabled in mode register 2; Mode details: see Table 7-9
IDDQ5C	Burst refresh IDDQ5C current (same bank refresh mode) Same conditions as IDD5C, but measuring IDDQ current instead of IDD current
IPP5C	Burst refresh IPP5C current (same bank refresh mode) Same conditions as IDD5C, but measuring IPP current instead of IDD current

Symbol	Description
IDD6N	Self-refresh current: Normal temperature range TCASE: 0 - 85°C; External clock: Off; CK_t and CK_c: HIGH; tCK, nCPDED: See Chapter 9.3 for timing parameters of each speed grade; BL:161; CS_n#: Low; CA, DQ: High; DM_n: High; Memory Activity: Self-Refresh Operation; Output buffers: Disabled; ODT: All ODTs disabled in MR32–MR35;
IDDQ6N	Self-refresh IDDQ current: Normal temperature range Same conditions as IDD6N, but measuring IDDQ current instead of IDD current
IPP6N	Self-refresh IPP current: normal temperature range Same conditions as IDD6N, but measuring IPP current instead of IDD current
IDD6E	Self-refresh current: extended temperature range (case temperature: 85 - 95°C); external clock: off; CK_t and CK_c: high; tCK, nCPDED: refer to Section 9.3 "Timing Parameters by Speed Grade"; BL:161; CS_n: low; CA, data input/output: high; DM_n: stable at 1; Memory Activity: Self-Refresh Operation; Output Buffers and RTT: Enabled in Mode Register 2
IDDQ6E	Self-Refresh IDDQ Current: Extended Temperature Range Same conditions as IDD6E, but measuring IDDQ current instead of IDD current
IPP6E	Self-Refresh IPP Current: Extended Temperature Range Same conditions as IDD6E, but measuring IPP current instead of IDD current
IDD7	Operating Row Interleave Read Current; External Clock: On; tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S: Refer to Section 9.3 "Timing Parameters by Speed Grade"; BL:161; CS_n: at high level between ACT and RDA; CA inputs: partially toggling per Table 7-11; Data I/O: read data bursts per Table 7-11, data different between consecutive bursts; DM_n: stable at 1; Bank activity: cycling through banks (0,1,...7) twice with different addressing (see Table 7- 11); output buffers and RTT: enabled in Mode Register 2; Mode details: see Table 7-11
IDDQ7	Operating bank interleave read IDDQ current Same conditions as IDD7, but measuring IDDQ current instead of IDD current
IPP7	IPP current during inter-bank read Same conditions as IDD7, but measuring IPP current instead of IDD current

IDD8	Maximum power-saving deep power-down current; External clock: off; CK_t and CK_c: HIGH; tCK, nCPDED: See timing parameters for different speed grades in Chapter 9.3; BL:161; CS_n: LOW; CA: HIGH; DM_n: steady at 1; Bank activity: All banks closed, device in MPSM deep power-down mode 5; Output buffer and RTT: enabled in mode register 2; Mode details: Same as IDD6N, but MPSM enabled in mode register.
IDDQ8	Maximum power-down deep sleep IDDQ current Same conditions as IDD8, but measuring IDDQ current instead of IDD current
IPP8	Maximum power-down deep sleep IPP current Same conditions as IDD8, but measuring IPP current instead of IDD current
IDD9 (optional)	MBIST current Device in MBIST mode, external clock: on; CS_n: Stays at 1 after entering MBIST; CA inputs: Stays at 1; Data I/O: VDDQ level; Memory bank activity: MBIST operation; Output buffer: enabled via MR5; RTT: enabled via MR2.
IDDQ9 (Optional)	MBIST IDDQ current Same conditions as IDD9, but measuring IDDQ current instead of IDD current
IPP9 (Optional)	MBIST IPP current Same conditions as IDD9, but measuring IPP current instead of IDD current

Note 1: Burst length: BL16 is fixed by MR0
OP[1:0]=00. Note 2: Output buffer enable: set MR5
OP[0]=0: Qoff = output buffer enabled; set MR5
OP[2:1]=00: pull-up output driver impedance
control = RZQ/7.
Set MR5 OP[0]=0: Qoff = output buffer enabled.
Set MR5 OP[2:1]=00: pull-up output driver impedance control = RZQ/7.
Set MR5 OP[7:6]=00: pull-down output driver impedance control = RZQ/7.
RTT_Nom enable: set MR35 OP[5:0]=110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6. RTT_WR
enable: set MR34 OP[5:3]=010: RTT_WR = RZQ/2.
CA/CS/CK ODT, DQS_RTT_PART and RTT_PARK
disable: set MR32 OP[5:0]=000000.
Set MR33 OP[5:0]=000000.
Set MR34 OP[2:0]=000.
Note 3: Write CRC enabled, set MR50 OP[2:1]=11
Note 4: Read CRC enabled, set MR50 OP[0]=1
Note 5: MPSM deep power-down mode
Set MR2 OP[3]=1 (if PDA enumeration ID is not
equal to 15); set MR2 OP[5]=1 (if PDA enumeration
ID is equal to 15)

7.2 IDD0, IDDQ0, IPP0 modes

When executing all bank and bank group addresses, perform active and precharge commands with the strictest timing. Note 2 applies to the entire table.

Table 7-2 IDD0, IDDQ0, IPP0

Sub-cycle	Sequence	Command	CS_n	C/A [13:0]	Row Address[17:0]	Column Address[1:0]	BG[2:0]	CID [2:0]	Special Command
0	0	ACT	L	-	0x00000	0x0	0x00	0x0	
			H						
	1	DES	H	Toggle 1					Repeat sequence to satisfy tRAS(min), truncate if necessary
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggle 1					Repeat sequence to satisfy tRP(min), truncate if necessary
	4	ACT	L	-	0x03FFF	0x0	0x00	0x0	
			H						
	5	DES	H	Toggle 1					Repeat sequence to satisfy tRP(min), truncate if necessary
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggle 1					Repeat sequence to satisfy tRP(min), truncate if necessary
1	8-15	Repeat sub-cycle 0, using BG[2:0]=0x1							
2	16-23	Repeat sub-cycle 0, using BG[2:0]=0x2							
3	24-31	Repeat sub-cycle 0, using BG[2:0]=0x3							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							Skip x16
5	40-47	Repeat sub-cycle 0, using BG[2:0]=0x5							Skip x16
6	48-55	Repeat sub-loop 0, using BG[2:0]=0x6							Skip x16
7	56-63	Repeat sub-loop 0, using BG[2:0]=0x7							Skip x16
8-15	64-127	Repeat sub-loops 0-7, using BA[1:0]=0x1							
16-23	128-191	Repeat sub-loops 0-7, using BA[1:0]=0x2							
24-31	192-255	Repeat sub-loops 0-7, using BA[1:0]=0x3							
....	....	If applicable, repeat sub-loops 0-31 for each 3DS logic level							CID[2:0]=0x1-0x7
Note 1: When toggling all C/A bits in the 4-cycle sequence defined by IDD2N and IDD3N modes, a DESELECT command must be inserted between commands. Note 2: For 3DS, all banks at the 'non-target' logic level use IDD2N conditions.									

7.3 IDD0F, IDDQ0F, IPP0F Modes

Rolling activation and precharge of four banks per tRC cycle, covering all banks, bank groups, and CID addresses. Note 2 applies to the entire table.

Table 7-3 IDD0F, IDDQ0F, IPP0F

Sub-cycle	Sequence	Command	CS_n	Control/Address[13:0] [13:0]	Row Address[17:0]	Column Address[1:0]	BG[2:0]	CID [2:0]	Special Command
0	0	ACT	L		0x00000	0x0	0x00	0x0	
			H						
	1	DES	H	Toggle 1					Repeat operation to meet tRRD(min) requirement (7 DES operations needed to achieve 8nCK standard)
	2	ACT	L		0x00000	0x0	0x01	0x0	
			H						

	3	DES	H	Toggle 1					Repeat operations to meet tRRD(min) requirement (requires 7 DES commands to meet the 8nCK criteria)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggle 1					Repeat operations to meet tRRD(min) requirement (requires 6 DES commands to meet the 8nCK criteria)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggle 1					Repeat the tRAS(min) requirement from Sequence 0 tRAS(min) requirement
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggle 1					Repeat tRRD(min) operation (7 DES commands to meet 8nCK), which allows the next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggle 1					Repeat tRRD(min) (requires 7 DES to reach 8nCK). This operation provides the condition for the subsequent tRAS(min) requirement; PRE meets tRAS(min).
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggle 1					Repeat tRRD(min) operation (7 DES to reach 8nCK). This enables the next PRE to satisfy tRAS(min).
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggle 1					Repeat tRRD(min) operation (7 DES to reach 8nCK). This enables the next PRE to satisfy tRAS(min).
	16	DES	H	Toggle 1					Repeat tRC(min) starting from the first activation of sub-loop 0.
1	17-33	Repeat sub-cycle 0, using row address = 0x03FFF as the ACT address							
2-3	34-67	Repeat sub-cycles 0–1, replace BG[2:0]=0x4,0x5,0x6,0x7 with 0x0,0x1,0x2,0x3							Skip x16
4-7	68-101	Repeat sub-cycles 0–3, using BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-cycles 0–3, change to BA[1:0]=0x2							
12-15	136-169	Repeat sub-cycles 0–3, change to BA[1:0]=0x3							
...	...	If applicable, repeat sub-cycles 0–15 for each 3DS logic level							CID[2:0]=0x1-0x7
Note 1: When toggling all C/A bits in the 4-cycle sequence defined by IDD2N and IDD3N modes, a DESELECT command must be used between commands. Note 2: For 3DS, all banks in all 'non-target' logic levels are in IDD2N state.									

7.4 IDD2N and IDD3N modes

All command/address pins are operated while executing DESELECT commands in the predefined modes. All notes apply to the entire datasheet.

Table 7-4 IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF
Note 1: Data is pulled to VDDQ Note 2: DQS_t and DQS_c are pulled to VDDQ NOTE 3: Command/Address ODT is disabled. NOTE 4: Repeat sequences 0 to 3. NOTE 5: All memory cells at all logic levels simulate identical test conditions.			

7.5 IDD2NT, IDDQ2NT, IPP2NT Modes

Execute non-target write command, simulate inter-rank timing, while testing all C/A bits. Notes 3-6 apply to the entire table.

Table 7-5 IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Command
0	WRITE1	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggle 2	Repeat pattern to meet 1*tCCD_S(min), truncate if necessary
2	WRITE1	WRITE1	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggle 2	Repeat pattern to meet 1*tCCD(min), truncate as required
Note 1: Write operations with CS_n = L for two clock cycles are considered non-target writes. Note 2: When switching C/A bits, use DESELECT between commands, following the 4-cycle sequence defined in IDD2N and IDD3N patterns. Note 3: The non-target write interval reflects a single rank tCCD_S(min). Note 4: DQ signals are at VDDQ. Note 5: DQS_t and DQS_c are at VDDQ. Note 6: Repeat 0 to 3				

7.6 IDD4R, IDDQ4R, IPP4R Patterns

While activating all banks, bank groups, and CID addresses, execute READ commands with the tightest timing. Notes 2–9 apply to the entire table.

Table 7-6 IDD4R, IDDQ4R, IPP4R

Sub-cycle	Sequence	Command	CS_n	Control/ Address [13:0]	Row Address[17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16) (BL=16)	Special Command
0	0	Read	Read H	-	0x000	0x00	0x0	0x0	Mode A	All "valid" inputs = VDDQ
	1	DES	H	Toggle 1						Repeat sequence to satisfy tCCD_S(min), truncate if necessary
1	2	Read	L H	-	0x3F0	0x00	0x01	0x0	1	All "valid" inputs = VDDQ
	3	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
2	4-5	Repeat subcycle 0, set BG[2:0]=0x2								
3	6-7	Repeat subcycle 1, set BG[2:0]=0x3								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								Skip x16
5	10-11	Repeat subcycle 1, set BG[2:0]=0x5								Skip x16
6	12-13	Repeat subcycle 0, set BG[2:0]=0x6								Skip x16
7	14-15	Repeat Sub-loop 1, set BG[2:0]=0x7								Skip x16
8	16	Read	Read H	-	0x3F0	0x00	0x0	0x0	Mode B	All "valid" inputs = VDDQ
	17	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
9	18	Read	Read H	-	0x000	0x00	0x01	0x0	Mode A	All "valid" inputs = VDDQ
	19	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
10	20-21	Repeat sub-loop 8, set BG[2:0]=0x2								
11	22-23	Repeat Sub-cycle 9, using BG[2:0]=0x3								
12	24-25	Repeat Sub-cycle 8, using BG[2:0]=0x4								Skip x16
13	26-27	Repeat Sub-cycle 9, using BG[2:0]=0x5								Skip x16
14	28-29	Repeat Sub-cycle 8, using BG[2:0]=0x6								Skip x16
15	30-31	Repeat subcycle 9, using BG[2:0]=0x7								Skip x16
16-31	32-33	Repeat subcycles 0-15, using BA[1:0]=0x1								
32-47	34-35	Repeat subcycles 0-15, using BA[1:0]=0x2								
48-63	36-37	Repeat subcycles 0-15, using BA[1:0]=0x3								
...	...	If applicable, repeat subcycles 0-63 for each 3DS logic rank								CID[2:0]=0x1-0x7

NOTE 1: When toggling all CA bits in the 4-cycle sequence defined by IDD2N and IDD3N modes, insert DESELECT commands between commands. NOTE 2: When performing a READ operation, auto precharge = H.
NOTE 3: Row address set to 0x0000
NOTE 4: Data reflects burst length of 16.
NOTE 5: x4 data pattern A: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF. NOTE 6: x4 data pattern B: 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0xF, 0x0. NOTE 7: x8 data pattern: each byte consists of two identical nibbles (data pattern A = 0x00, 0xFF, 0xFF...).
Note 8: The x16 data pattern will present two identical bytes per beat (Data Pattern A: = 0x0000, 0xFFFF, 0xFFFF...).
Note 9: When the C/A column is not filled, refer to the Command Truth Table, Column Address, BA, BG, and CID to determine the C/A state.

7.7 IDD4W, IDDQ4W, IPP4W Modes

When executing WRITE commands across all banks, bank groups, and CID addresses, use the tightest timing. Notes 2-6 apply to the entire table.

Table 7-7 IDD4W, IDDQ4W, IPP4W

Sub-cycle	Sequence	Command	CS_n	Control/Address[13:0] [13:0]	Row Address[17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Command
0	0	WRITE	WRITE	-	0x000	0x00	0x0	0x0	Mode A	All "valid" inputs = VDDQ
			H							
	1	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
1	2	WRITE	L	-	0x3F0	0x00	0x01	0x0	Mode B	All "valid" inputs = VDDQ
			H							
	3	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
2	4-5	Repeat sub-loop 0, change BG[2:0]=0x2								
3	6-7	Repeat sub-loop 1, change BG[2:0]=0x3								
4	8-9	Repeat subcycle 0, using BG[2:0]=0x4 instead								Skip x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								Skip x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								Skip x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								Skip x16
8	16	WRITE	WRITE	-	0x3F0	0x00	0x0	0x0	Mode B	All "valid" inputs = VDDQ
			H							
	17	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
9	18	WRITE	L	-	0x000	0x00	0x01	0x0	Mode A	All "valid" inputs = VDDQ
			H							
	19	DES	H	Toggle 1						Repeat sequence to meet tCCD_S(min), truncate if necessary
10	20-21	Repeat Sub-cycle 8, using BG[2:0]=0x2								
11	22-23	Repeat Sub-cycle 9, using BG[2:0]=0x3								
12	24-25	Repeat Sub-cycle 8, using BG[2:0]=0x4								Skip x16
13	26-27	Repeat Sub-cycle 9, using BG[2:0]=0x5								Skip x16
14	28-29	Repeat Sub-cycle 8, using BG[2:0]=0x6								Skip x16
15	30-31	Repeat subcycle 9, using BG[2:0]=0x7								Skip x16
16-31	32-33	Repeat subcycles 0-15, using BA[1:0]=0x1								
32-47	34-35	Repeat subcycles 0-15, using BA[1:0]=0x2								
48-63	36-37	Repeat subcycles 0-15, using BA[1:0]=0x3								
...	...	If applicable, repeat subcycles 0-63 for each 3DS logic rank								CID[2:0]=0x1-0x7

Note 1: The 4-cycle sequence defined by IDD2N and IDD3N modes uses DESELECT between commands. Note 2: WRITE operation must satisfy: Auto Precharge = H, Burst Chop = H.
Note 3: Row address set to 0x0000. Note 4: Data reflects burst length 16. Note 5: For data pattern definition, refer to the IDD4R measurement cycle table.
Note 6: When the C/A column is not filled, refer to the command truth table, column address, BA, BG, and CID to determine the C/A status.

7.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F modes

Execute refresh (all banks) command at minimum tRFC. Notes 3-6 apply to the entire table.

Table 7-8: IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS	C/A [13:0]	CA[9:8]	CID [2:0]	Special Notes
0	REFab	L	-	H	0x0	All "valid" inputs = VDDQ
1	DES	H	Toggle 1	-	-	Repeat sequence to meet tRFC(min) (Note 2) requirement, truncate if necessary.
2	REFab	L	-	H	0x0	All "valid" inputs = VDDQ
3	DES	H	Toggle 1	-	-	Repeat sequence to meet tRFC(min) (Note 2) requirement, truncate if necessary.
....	Repeat sequences 0-3 for each 3DS logical rank (if applicable).					CID[2:0]=0x1-0x7

Note 1: 4-cycle sequence as defined by IDD2N, IDD3N patterns, using DESELECT between commands. Note 2: IDD5B uses tRFC1(min), IDD5F uses tRFC2(min).
Note 3: DQ signals are at VDDQ.
Note 4: All non-target memory banks are in Idd2N condition.
Note 5: When the C/A [13:0] column is left blank, refer to the Command Truth Table, CA[9:8] column, and CID column to determine the C/A state. Note 6: When executing the REFab command on a device supporting RIR, CA8 must be set to H to indicate 1X refresh rate.

7.9 IDD5C, IDDQ5C, and IPP5C Modes

Execute refresh (same bank) command with minimum tRFCsb. Notes 2-5 apply to the entire table.

Table 7-9 - IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS	C/A [13:0]	CA[9:8]	BA [1:0]	CID [2:0]	Special Notes
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggle 1	-		-	Repeat sequence to meet tRFCsb(min), truncate if necessary.
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggle 1	-		-	Repeat sequence to meet tRFCsb(min), truncate if necessary.
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggle 1	-		-	Repeat sequence to satisfy tRFCsb(min) condition, truncate if necessary
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggle 1	-		-	Repeat sequence to meet tRFCsb(min), truncate if necessary.
....	Repeat sequences 0-3 for each 3DS logical rank (if applicable).						CID[2:0]=0x1-0x7

Note 1: Use DESELECT command between commands per the 4-cycle sequence defined in IDD2N and IDD3N modes. Note 2: DQ signals are at VDDQ level.
Note 3: All memory banks of all non-target logical ranks are in IDD2N state.
Note 4: When the C/A[13:0] column is not filled, refer to the command truth table, CA[9:8], and CID columns to determine the C/A state. Note 5: All banks of all non-target logical ranks are in IDD2N state.

7.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R modes

All notes apply to the entire table.

Table 7-10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R modes

Sequence	Command	Clock	CS	CA[13:0]	Special Command
0	SRE	Valid	L	0x3BF7	tCKLCS(min)
1	DES	Valid	H	0x3FFF	Repeat sequence to meet tCPDED(min), truncate if necessary
2	All CA=H	Valid	L	0x3FFF	
3	All CA=H	CK_t= CK_c= H	L	0x3FFF	Repeat infinite sequence

Note 1: Data is pulled to VDDQ
Note 2: DQS_t and DQS_c are pulled to VDDQ
Note 3: For 3DS devices, all memory cells of all logical ranks simulate the same test conditions.

7.11 IDD7, IDDQ7, and IPP7 Test Mode

Execute ACTIVATE, READ with Auto-precharge commands with the tightest timing, while covering all bank, bank group, and CID addresses. Notes 2-6 apply to the entire table.

Table 7-11 IDD7, IDDQ7, IPP7

Sub Sequence	Sequence	Command	CS_n	C/A [13:0]	Row Address[17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Command
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0		
	1	DES	H	Toggle 1							Repeat sequence to satisfy tRRD_S(min)
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0		
	3	DES	H	Toggle 1							Repeat sequence to satisfy tRRD_S(min)
2	4-5		Repeat sub-loop 0, change BG[2:0]=0x2								
3	6-7		Repeat sub-loop 1, change BG[2:0]=0x3								
4	8-9		Repeat sub-loop 0, use BG[2:0]=0x4 instead								Skip x16
5	10-11		Repeat sub-loop 1, use BG[2:0]=0x5 instead								Skip x16
6	12-13		Repeat sub-loop 0, use BG[2:0]=0x6 instead								Skip x16
7	14-15		Repeat sub-loop 1, use BG[2:0]=0x7 instead								Skip x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Mode A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggle 1							Repeat sequence to satisfy tCCD_S(min)
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Mode B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
				Toggle 1							Repeat sequence to satisfy

	21	DES	H							tCCD_S(min)
10	20-24	Repeat sub-cycle 8, using BG[2:0]=0x2 instead								
11	25-27	Repeat sub-cycle 9, using BG[2:0]=0x3 instead								
12	28-30	Repeat sub-loop 8, change BG[2:0] to 0x4								Skip x16
13	31-33	Repeat sub-loop 9, change BG[2:0] to 0x5								Skip x16
14	34-36	Repeat sub-loop 8, change BG[2:0] to 0x6								Skip x16
15	37-39	Repeat sub-loop 9, change BG[2:0] to 0x7								Skip x16
16-23	40-64	Repeat sub-loops 8-15, RDA uses BA[1:0]=0x1, ACT uses BA[1:0]=0x2								
24-31	65-89	Repeat sub-loops 8-15, RDA uses BA[1:0]=0x2, ACT uses BA[1:0]=0x3								
32-39	90-114	Repeat sub-loops 8-15, RDA uses BA[1:0]=0x3, ACT uses BA[1:0]=0x0								
.....	...	If applicable, repeat sub-loops 0-18 for each 3DS logic rank.								CID[2:0]=0x1-0x7

Note 1: 4-cycle sequence as defined in IDD2N and IDD3N patterns, using DESELECT between commands. Note 2: When performing READ operation, auto precharge = L, burst chop = H.
Note 3: x8 or x16 mode may have different bank or bank group addresses. Note 4: Data reflects 16-byte burst length.
Note 5: For data pattern definitions, refer to the IDD4R measurement loop table.
Note 6: For 3DS, all banks of all 'non-target' logic ranks are in IDD2N state.

7.12 IDD Specifications

The measurement and classification of DDR5 SDRAM current limits are performed according to the definitions in the DDR5 product core datasheet. For detailed information on each current limit, refer to the IDD and IDDQ specifications and test conditions.

The maximum IDD current considers worst-case process, temperature, and voltage conditions.

Table 7-12 IDD and IDDQ Specifications

Type	Symbol	4800			5600			6400			Unit
		x4	x8	x16	x4	x8	x16	x4	x8	x16	
IDD0	IDD0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD0F	IDD0F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ0F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP0F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD2	IDD2N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ2N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP2N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD2NT	IDD2NT	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ2NT (Optional)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP2NT (optional)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD2P	IDD2P	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ2P	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP2P	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD3N	IDD3N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ3N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP3N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD3P	IDD3P	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ3P	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP3P	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDD4R	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDD4RC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA

IDD4R	IDDQ4R	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ4RC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP4R	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP4RC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD4W	IDD4W	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDD4WC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ4W	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ4WC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP4W	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP4WC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD5B	IDD5B	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ5B	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP5B	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD5F	IDD5F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ5F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP5F	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD5C	IDD5C	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ5C	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP5C	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD6N	IDD6N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ6N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP6N	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD6E	IDD6E	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ6E	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP6E	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD7	IDD7	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ7	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP7	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD8	IDD8	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ8	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP8	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD9	IDD8 (optional)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IDDQ8 (Optional)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	IPP8 (optional)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA

8. Input/Output Capacitance

Table 8-1 Chip I/O Capacitance DDR5-4800/5600/6400

Symbol	Parameter	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Note
		Min	Max	Min	Max	Min	Max		
Maximum	Input/Output Capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.40	0.9	0.40	0.85	0.40	0.8	pF	1,2
CDIO	Input/Output Capacitance Delta (DQ, DM) (DQ, DM_n)	-0.1	0.1	-0.1	0.1	-0.1	0.1	p F	1,2,8
CDDQS	Input/Output Capacitance Delta (DQS_t and DQS_c)	-	0.04	-	0.04	-	0.04	p F	1,2,4
CCK	Input Capacitance (CK_t and CK_c) CK_c)	0.2	0.6	0.2	0.55	0.2	0.5	p F	1,2
CDCK	Input capacitance delta (CK_t and CK_c)	-	0.05	-	0.05	-	0.05	p F	1,2,3
CI	Input capacitance (CS_n and CA[13:0] pins)	0.2	0.6	0.2	0.5/0.55	0.2	0.5	p F	1,2,5
CDI_ CS_n	Input capacitance delta (CS_n pin only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	p F	1,2,6
CDI_ CA	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	p F	1,2,7
CALERT	Input/Output ALERT capacitance	0.4	1.5	0.4	1.5	0.4	1.5	p F	1,2
Loopback	Loopback input/output capacitance (LBDQ, LBDQS)	0.3	1.0	0.3	1.0	0.3	1.0	p F	1,2
CTEN	TEN input capacitance	0.2	2.3	0.2	2.3	0.2	2.3	p F	1,2,9
CZQ	ZQ input capacitance	-	5	-	5	-	5	p F	1,2,11
CSTRAP	MIR, CAI, CA_ODT input capacitance	-	10	-	10	-	10	p F	1,2,10

Note 1: This parameter is not subject to production test. It is measured using vendor-specific measurement methods. Note 2: This parameter applies only to single-die devices; stacked/dual-die devices are excluded.
Note 3: Absolute value of CIO(CK_t) - CIO(CK_c) Note 4: Absolute value of CIO(DQS_t) - CIO(DQS_c) Note 5: CI applies to CS_n and CA[13:0]
Note 6: CDI_CS_n = CI(CS_n) - 0.5*(CI(CK_t) + CI(CK_c)) Note 7: CDI_CA = CI(CA[13:0]) - 0.5*(CI(CK_t) + CI(CK_c)) Note 8: CDIO = CIO(DQ, DM) - Avg(CIO(DQ, DM))
Note 9: The TEN pin may be internally pulled to VSS through a weak pull-down resistor. At that time, CTEN may be invalid. The system must verify the TEN signal according to supplier-specific information.

Table 8-2 DRAM Package Electrical Specifications (x4/x8)

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input/Output Zpkg	Zpkg_DQ	45	75	50	75	50	75	Ω	1,2,4,5,10
Input/Output Package Delay	Tpkg_delay_DQ	10	35	10	32	10	32	ps	1,3.4.5.10
DQS_t, DQS_c Zpkg	Zpkg_DQS	45	75	50	75	50	75	Ω	1,2,5,10,12
DQS_t, DQS_c package delay	Tpkg_delay_DQS	10	35	10	232	10	232	ps	1,3.5.10.12
Delta Zpkg DQS_t, DQS_c	DZpkg_DQS	-	5	-	5	-	5	Ω	1,2,5,7,10
Differential delay DQS_t, DQS_c	DTpkg_delay_DQS	-	2	-	2	-	2	ps	1,3,5,7,10
Input - CTRL pin Zpkg	Zpkg_CTRL	45	75	45	75	45	75	Ω	1,2,5.9.10
Input - CTRL pin package delay	Tpkg_delay_CTRL	10	35	10	28	10	28	ps	1,3,5.9.10
Input - CMD/ADD pin Zpkg	Zpkg_CA	45	75	45	75	45	75	Ω	1,2,5,8,10
Input - CMD/ADD pin package delay	Tpkg_delay_CA	10	35	10	35/32/29	10	35/32/29	ps	1,3,5,8,10
CK_t & CK_c Zpkg	Zpkg_CK	45	75	45	75	45	75	Ω	1,2,5,10
CK_t & CK_c package delay	Tpkg_delay_CK	10	30	10	25	10	25	ps	1,3,5,10
Delta Zpkg CK_t, CK_c	DZpkg_delay_CK	-	5	-	5	-	5	Ω	1,2,5,6,10
Delta delay CK_t and CK_c	DTpkg_delay_CK	-	2	-	2	-	2	ps	1,3,5,6,10
ALERT Zpkg	Zpkg_ALERT	45	75	45	75	45	75	Ω	1,2,5,10
ALERT delay	tpkg_delay_ALERT	10	60	10	60	10	60	ps	1,3,5,10
Loopback Zpkg	Zpkg_loopback	45	75	45	75	45	75	Ω	1,2,5,10,11
Loopback delay	tpkg_delay_Loopback	10	60	10	60	10	60	ps	1,3,5,10,11

Note 1: This parameter is not required for production testing.
Note 2: This parameter is measured using a vendor-specific method by averaging the Zpkg_xx values over the Tpkg_delay_xx time interval. Note 3: This parameter is measured using a vendor-proprietary measurement method.
Note 4: Zpkg_DQ and Tpkg_delay_DQ apply to DQ and DM.
Note 5: This parameter applies only to single-die devices; it does not cover stacked/dual-die devices.
Note 6: Absolute value of Zpkg_CK_t - Zpkg_CK_c for impedance (Z), or absolute value of Tpkg_delay_CK_t and Tpkg_delay_CK_c for delay (Tpkg_delay). Note 7: Absolute value of Zpkg(DQS_t) - Zpkg(DQS_c) for impedance (Z), or absolute value of Tpkg_delay_DQS_t - Tpkg_delay_DQS_c for delay (Tpkg_delay). Note 8: Zpkg_CA and Tpkg_delay_CA apply to CA[13:0].
Note 9: Zpkg_CTRL and Tpkg_delay_CTRL apply to CS_n.
Note 10: If the designed Zpkg and Tpkg_delay are within the ranges shown, the package implementation shall meet the specification. Note 11: Zpkg_Loopback and Tpkg_delay_Loopback apply to LBDQ and LBDQS.
Note 12: Zpkg_DQS and Tpkg_delay_DQS apply to DQS_t and DQS_c, TDQS_t and TDQS_c

Table 8-3 DRAM Package Electrical Specifications (X16)

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input/Output Zpkg	Zpkg_DQ	45	75	TBD	TBD	TBD	TBD	Ω	1,2,4,5,10
Input/Output Package Delay	Tpkg_delay_DQ	10	40	TBD	TBD	TBD	TBD	ps	1,3.4.5.10
DQS_t, DQS_cZpkg	Zpkg_DQS	45	75	TBD	TBD	TBD	TBD	Ω	1,2,5,10,12
DQS_t, DQS_c package delay	Tpkg_delay_DQS	10	40	TBD	TBD	TBD	TBD	ps	1,3.5.10.12
Delta Zpkg DQS_t, DQS_c	DZpkg_DQS	-	5	TBD	TBD	TBD	TBD	Ω	1,2,5,7,10
Delta Delay DQS_t, DQS_c	DTpkg_delay_DQS	-	2	TBD	TBD	TBD	TBD	ps	1,3,5,7,10
Input - CTRL pin Zpkg	Zpkg_CTRL	45	75	TBD	TBD	TBD	TBD	Ω	1,2,5.9.10
Input - CTRL pin package delay	Tpkg_delay_CTRL	10	40	TBD	TBD	TBD	TBD	ps	1,3,5.9.10
Input - CMD/ADD pin Zpkg	Zpkg_CA	45	75	TBD	TBD	TBD	TBD	Ω	1,2,5,8,10
Input - CMD/ADD pin package delay	Tpkg_delay_CA	10	45	TBD	TBD	TBD	TBD	ps	1,3,5,8,10
CK_t & CK_cZpkg	Zpkg_CK	45	75	TBD	TBD	TBD	TBD	Ω	1,2,5,10
CK_t & CK_c package delay	Tpkg_delay_CK	10	45	TBD	TBD	TBD	TBD	ps	1,3,5,10
Delta Zpkg CK_t & CK_c	DZpkg_delay_CK	-	5	TBD	TBD	TBD	TBD	Ω	1,2,5,6,10
ΔtCK_pkg	ΔtCK_pkg	-	2	TBD	TBD	TBD	TBD	ps	1,3,5,6,10
ALERT Zpkg	Zpkg_ALERT	45	75	TBD	TBD	TBD	TBD	Ω	1,2,5,10
ALERT delay	Tpkg_delay_ALERT	10	60	TBD	TBD	TBD	TBD	ps	1,3,5,10
Loopback Zpkg	Zpkg_loopback	45	75	TBD	TBD	TBD	TBD	Ω	1,2,5,10,11
Loopback delay	Tpkg_delay_LB	10	60	TBD	TBD	TBD	TBD	ps	1,3,5,10,11

Note 1: This parameter is not required for production testing.
Note 2: This parameter is obtained using a supplier-specific measurement method by calculating the average Zpkg_xx value over the interval Tpkg_delay_xx. Note 3: This parameter is measured using a supplier-specific measurement method. Note 4: Zpkg_DQ & Tpkg_delay_DQ apply to DQ and DM.
Note 5: This parameter applies only to single-die devices; it does not cover stacked/dual-die devices.
Note 6: Absolute value of Zpkg_CK_t - Zpkg_CK_c for impedance (Z), or absolute value of Tpkg_delay_CK_t - Tpkg_delay_CK_c for delay (Tpkg_delay).
Note 7: Impedance (Z) is the absolute value of Zpkg_DQS_t - Zpkg_DQS_c, or delay (Tpkg_delay) is the absolute value of Tpkg_delay_DQS_t - Tpkg_delay_DQS_c. Note 8: Zpkg_CA and Tpkg_delay_CA apply to CA[13:0].
Note 9: Zpkg_CTRL and Tpkg_delay_CTRL apply to CS_n.
Note 10: If the design Zpkg and Tpkg_delay are within the indicated ranges, the package implementation shall meet the specification.
Note 11: Zpkg_Loopback and Tpkg_delay_Loopback apply to LBDQ and LBDQS.
Note 12: Zpkg_DQS and Tpkg_delay_DQS apply to DQS_t and DQS_c, TDQS_t and TDQS_c.

8.1 Electrostatic Discharge Sensitivity Characteristics

Table 8-4 Electrostatic Discharge Sensitivity Characteristics

Parameter 1	Symbol	Min	Max	Unit	Notes
Human Body Model (HBM)	ESDHBM	1000	-	V	2
Charged Device Model (CDM)	ESDCDM	250	-	V	3
Note 1: Standard ESD control measures must be implemented when handling devices. Note 2: Refer to ESDA/JEDEC Joint Standard JS-001 for measurement procedures. Note 3: Refer to ESDA/JEDEC Joint Standard JS-002 for measurement procedures.					

9. Electrical Characteristics and AC Timing

9.1 Reference Load for AC Timing and Output Slew Rate

Figure 9-1 shows the 50-ohm effective reference load used to define the device's AC timing parameters and output slew rate measurements.

The nominal RON of the DQ, DQS_t, and DQS_c drivers is 34 ohms for specifying the device's AC timing parameters.

- The maximum DC high level of the output signal is 1.0*VDDQ,
- The DC low level minimum of the output signal is {34/(34+50)}*VDDQ, and the DC high level maximum is 0.4*VDDQ
- The nominal reference level of the output signal can be approximated as follows:
- Midpoint of DC high-level maximum and DC low-level minimum = { (1+0.4)/2 } * VDDQ = 0.7 * VDDQ

The actual reference level of the output signal may vary due to driver on-resistance (RON) and reference load tolerance. Therefore, the actual reference level or midpoint of the output signal is located at the widest part of the output signal eye diagram. Before measuring AC parameters, set the reference level of the verification tool to an appropriate value.

This design is not intended to accurately represent a specific system environment, nor does it describe the load applied by an actual production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load with the system environment. Manufacturers need to correlate it with production test conditions, typically using one or more coaxial transmission lines terminated to the tester electronics.

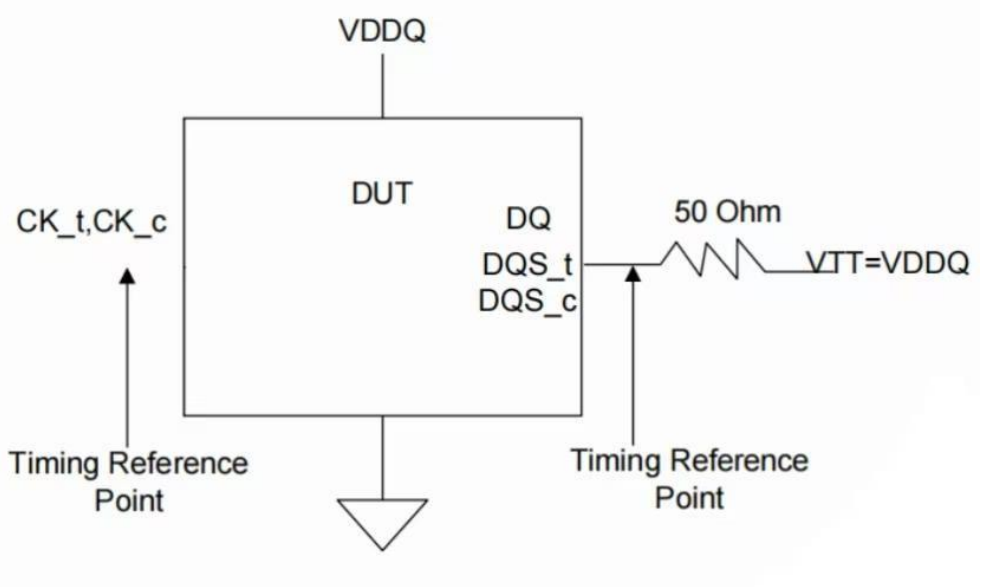


Figure 9-1 AC Timing and Output Slew Rate Reference Load

9.2 Rounding Definition and Algorithm

Software algorithms used to calculate timing parameters are affected by rounding errors from multiple sources. For example, a system may use a memory clock with a nominal frequency of 2200 MHz (4400 MT/s) for the DDR5-4400 speed grade, whose mathematically calculated clock period

tCK(AVG) is 0.454545... ns. In most cases, it is impossible to accurately represent all decimal places, so rounding must be applied. The DDR5 SDRAM specification sets a minimum precision requirement of 1 ps for timing parameters.
Rounding rules must be defined to optimize device performance without violating device parameters. All timing parameters defined in the time domain (ns, ps, etc.) should be defined following these rules when converting to the clock domain (nCK units). The key point is: minimum timing parameters should generally use the same rounding rules as those defined for tCK(AVG)min. The resulting rounding algorithm relies on results within the correction coefficient range of device testing and specifications to avoid performance loss due to rounding errors.
The specific rules are as follows:

- All minimum timing parameter values (including tCK(AVG)min) are rounded down and defined with 1 ps precision based on the unrounded nominal tCK(AVG)min value corresponding to the specified speed in the DDR5 SDRAM specification. If the nominal minimum timing parameter value requires precision greater than 1 ps, it can be rounded down (to a faster value) to the next 1 ps using the rounding algorithm, and the DDR5 SDRAM absorbs this tiny minimum parameter expansion. In other words, the DDR5 SDRAM specification only lists nominal minimum parameter values rounded to the nearest 1 ps. For example, this precisely extends the definition of DDR5-4400 tCK(AVG)min to

  0.454 ns, which is 1 ps less than the nominal memory clock cycle of 0.454545... ns (i.e., slightly faster).
- For other minimum timing parameters besides tCK(AVG)min, to avoid performance loss due to additional fractional nCK and to calculate the true minimum, the nominal values listed in the DDR5 SDRAM specification must be reduced (accelerated) by the same or greater percentage (correction factor) as used to define tCK(AVG)min. The DDR5 SDRAM absorbs these parameter expansions. For example, the nominal tWRmin is 30.000 ns, but applying a 0.30% correction factor can support more aggressive timing (such as 29.910 ns), thereby maintaining the expected smaller (faster) nCK value when tCK(AVG)min is rounded down to the nearest 1 ps. Note: Parameter values defined as 0 ps do not require correction factor adjustment and therefore are not subject to such rounding algorithms.
- When using real arithmetic, nominal minimum parameters such as tWRmin and tRCDmin, which are programmed in the system as clock cycle counts (nCK) but expressed in time units, must be divided by the actual memory clock cycle tCK(AVG)real to obtain the ratio in clock cycle counts (nCK), then multiplied by a correction factor of 99.70% (i.e., 1 - 0.30%), and finally rounded up to the nearest integer clock cycle:

$$nCK = ceiling[\frac{\text{parameter_nominal x } 0.997}{\text{tCK(AVG)real}}]$$

- In the industry, integer arithmetic with only downward rounding is commonly used when calculating nCK values. This second algorithm is implemented by scaling by a factor of 1000.

To achieve integer arithmetic: first multiply the nominal minimum parameter (in picoseconds) by the scaling correction factor (1000−3=997), then divide by the applied memory clock cycle;

- Then add 1 (which has been multiplied by 1000 for scaling) to the result, effectively rounding the result up. Dividing by 1000 removes the scaling.
  effect, finally resulting in a simple integer number of clock cycles. Note that the operation of effectively adding 1 before rounding down is essentially equivalent to rounding up, unless the result is exactly an integer (integer value), in which case the result will not round down as intended, leading to a performance penalty. To address this issue, the maximum correction factor of 0.28% required for 3600 MHz (7200 MT/s) operation is slightly increased to 0.30% in these rounding algorithms. This adjustment covers all integer boundary conditions, except when the nominal minimum timing parameter value is defined as 0 ps. This integer-only floor math rounding algorithm is neither necessary nor optimized for the 0 ps parameter value scenario, and its forced application would result in a performance penalty.

$$nCK = truncate[\frac{(\frac{truncate[\text{parameter_nominal_in_ps}]x997}{truncate[\text{tCK(AVG)_real_in_ps}]}) + 1000}{1000}]$$

- Both the real math rounding algorithm and the integer-only floor math rounding algorithm yield similar results. In the event of conflicting results, the integer-only floor math rounding algorithm takes precedence.
- When converting from the time domain (ns, picoseconds, etc.) to the clock domain (nCK units), all minimum timing parameters should use real math and integer-only floor math rounding algorithms, except for the conversion of tAA to CL. If these rounding algorithms are used to convert tAA to CL, invalid CL values may be returned in some cases during down-clock operations (and the DIMM SPD CL mask cannot fully avoid these situations). The correct CL setting should be determined by the memory controller, via the speed bin table, CL algorithm, or other methods. For more information, refer to the 'Speed Bins and Operation' section. Note: The CL algorithm can replace the use of the DIMM SPD CL mask.
- If the DDR5 SDRAM supports non-standard tCK, tAA, tRCD, and tRP speed bin timings, the CL algorithm still only returns valid CL values defined in the speed bin table, which may not be the expected CL values for the non-standard speed bin. In such cases, a rounding-up algorithm should be used to convert tAA to CL values, rather than the CL algorithm. According to the DIMM SPD CL mask, the rounded-up CL value should be taken to the next supported CL value. For more information, consult the memory supplier.

9.2.1 Example - Real Math

Converting tWR(min) from ns to nCK using real math:

The algorithm reduces the nominal minimum timing parameter values by a correction factor of 99.70% and rounds the nCK up to the nearest integer value:

real TwrMin, Correction, ClockPeriod, TempTwr, TempNck

```
int TwrInNck;
TwrMin = 30.000;                                    // tWRmin(ns)
Correction = 0.003                                  // According to the rounding algorithm, this is 0.30%
ClockPeriod = ApplicationTck;   // Clock period in ns is application-specific
TempTwr = TwrMin * (1 - Correction);   // Apply correction factor
TempNck = TempTwr / ClockPeriod;   // Initial nCK calculation
TwrInNck = (int) ceiling(TempNck);   // Round up to the next integer value
```

Table 9-1 Example 1 - Real Number Operations

DDR5 device timing parameters at standard application frequency: tWR(min) = 30.000ns					
Applied Speed Grade	Device tWR	Applied tCK	Device tWR / Applied tCK	Device tWR * (1 - Correction Value) / Application tCK	Ceiling Result
	ns	ns	nCK (Real)	nCK (Corrected)	nCK (Integer)
3200	30.000	0.625	48.00	47.86	48
3600	30.000	0.555	54.05	53.89	54
4000	30.000	0.500	60.00	59.82	60
4400	30.000	0.454	66.08	65.88	66
4800	30.000	0.416	72.12	71.90	72

9.2.2 Example 2 - Integer Operation

Converting tWR(min) from ns to nCK using integer arithmetic:

This algorithm reduces the nominal minimum timing parameter value by a 0.30% correction factor, adds 1 nCK, and rounds down nCK to the nearest integer.

```
int TwrMin, Correction, ClockPeriod, TempTwr, TempNck, TwrInNck;
TwrMin          =30000;                             // tWRmin (picoseconds)
CorrectionValue =3                                  // 0.30% according to rounding algorithm
ClockPeriod     = Application ClockPeriod;          // Clock period in picoseconds, depends on application
TempTwr         =TwrMin * (1000 - CorrectionValue); // Apply correction factor, scale by multiplying by 1000
TempNck         =TempTwr / ClockPeriod; // Initial nCK calculation, multiply by 1000

TempNck         =TempNck + 1000;                    // Add 1, multiplied by 1000, to achieve effective
rounding  TwrInNck                                  =(int)(TempNck / 1000);          // Round down to
the nearest integer
```

Table 9-2 Example 2 - Integer Arithmetic with Rounding Down

DDR5 device timing parameters when operating at standard application frequency: tWR(min) = 30.000 ns = 30000 ps					
Applied Speed Grade	Device tWR	Applied tCK	Device tWR / Applied tCK	Device tWR * (1000 - Correction) / Applied tCK tCK+ 1000	Corrected Truncated nCK / 1000
	ps	ps	nCK (Real)	nCK (Corrected)	nCK (Integer)
3200	30.000	625	48.00	48856	48
3600	30.000	555	54.05	54891	54
4000	30.000	500	60.00	60820	60
4400	30.000	454	66.08	66881	66
4800	30.000	416	72.12	72899	72

9.3 Timing Parameters by Speed Grade

The analog timing parameters in this section are defined based on nominal tCA(avg)min and following rounding rules. For details, refer to the 'Rounding Definition and Algorithm' section.

9.3.1 Timing Parameters for DDR5-3200 to DDR5-4000

Table 9-3 applies to DDR5-3200 to DDR5-4000

Speed		DDR5-3200		DDR5-3600		DDR5-4000		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock cycle									
Average Clock Period	tCK(avg)	0.625	-	0.555	-	0.500	-	ns	1
Command and address timing									
Read command delay (for the same bank group) bank group)	tCCD_L	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Write command delay for same bank group	tCCD_L_WR	max(32nCK,20ns)	-	Max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	nCK,ns	
Write command delay for same bank group, second write does not perform RMW	tCCD_L_WR2	max(16nCK,10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	nCK,ns	
Read-to-Write Command Delay (Same Bank Group)	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,ns	3,5,6
Write-to-Read Command Delay (Same Bank Group) bank group)	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read-to-Read Command Delay (Different Bank Groups)	tCCD_S	8	-	8	-	8	-	nCK	
Write-to-Read Command Delay (Different Bank Groups) Write-to-Write Command Delay (Different Bank Groups)	tCCD_S_WR	8	-	8	-	8	-	nCK	
Read-to-Write Command Delay (Different Bank Groups)	tCCD_S_RTWW	CL - CWL + RBL/2 + 2tCK - (read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,ns	3,5,6
Write-to-read command delay for different bank groups	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write-to-read command delay with auto precharge, same bank	tCCD_WTRA	CWL+ WBL/2 + tWR - tRTP						nCK,ns	2,4,6

Activate-to-activate command delay, same bank group, page size of 1KB	tRRD_S	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Activate-to-activate command delay, same bank group, page size of 2KB	tRRD_S(2K)	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Activate-to-activate command delay, different bank groups bank group, page size 1KB	tRRD_S(1K)	8	-	8	-	8	-	nCK	
Activate-to-Activate command delay, different bank group, 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	
Four Bank Activation Window, 1KB page size	tFAW (1K)	Max(32nCK, 20.000ns)	-	Max(32nCK, 17.777ns)	-	Max(32nCK, 16.000ns)	-	nCK, ns	
Four-Activation Window, 2KB Page Size	tFAW (2K)	Max(40nCK 40nCK, 25.000ns)	-	Max(40nCK, 22.222ns)	-	Max(40nCK, 20.000ns)	-	nCK, ns	
Read to Precharge Command Delay	tRTP	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to precharge command delay	tPPD	2	-	2	-	2	-	nCK	7
Write recovery time	tWR	30	-	30	-	30	-	ns	

9.3.2 Timing parameters for DDR5-4400 to DDR5-5200

The analog timing parameters in this section are defined based on nominal tCA(avg)min and following rounding rules. For details, refer to the 'Rounding Definition and Algorithm' section.

Table 9-4 DDR5-4400 to DDR5-5200 Specifications

Speed		DDR5-4400		DDR5-4800		DDR5-5200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock cycle									
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384	-	ns	1
Command and Address Timing									
Read-to-Read Command Delay within Same Bank Group	tCCD_L	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Write-to-Write Command Delay, Same Bank Group	tCCD_L_WR	max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	nCK,ns	
Write Command Delay (Same Bank Group), Second Write Without Read/Write	tCCD_L_WR2	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	nCK,ns	
Read-to-Write command delay (same bank group)	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,ns	3,5,6
Write-to-Read command delay (same bank group)	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read-to-Read command delay (different bank groups)	tCCD_S	8	-	8	-	8	-	nCK	
Write command delay (different bank groups) bank group)	tCCD_S_WR	8	-	8	-	8	-	nCK	
Read-to-Write command delay for different bank groups	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,ns	3,5,6

Write-to-Read command delay (for different bank groups) for different bank groups	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write-to-Read command delay with auto precharge to same bank Precharge command delay for same bank	tCCD_WTRA	CWL+ WBL/2 + tWR - tRTP						nCK,ns	2,4,6
Activate-to-Activate command delay (for 1KB page size same bank group) same bank group for 1KB page size	tRRD_L(1K)	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to same bank group, page size 2KB Activate to Activate command delay to same bank group, page size 2KB	tRRD_L(2K)	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Activate-to-Activate command delay, different bank groups 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	
ACTIVATE command delay to different bank group, page size 2KB ACTIVATE command delay to different bank group, page size 2KB	tRRD_S(2K)	8	-	8	-	8	-	nCK	
Four Bank Activation Window, 1KB page size	tFAW (1K)	MAX(32nCK, 14.545ns)	-	Max(32nCK, 13.333ns)	-	Max(32nCK, 12.307ns)	-	nCK, ns	
Four-Activation Window for 2KB Page Size	tFAW (2K)	Max(40nCK, 18.181ns)	-	Max(40nCK, 16.666ns)	-	Max(40nCK, 15.384ns)	-	nCK, ns	
Read to Precharge Command Delay	tRTP	Max (12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to precharge command delay	tPPD	2	-	2	-	2	-	nCK	7
Write recovery time	tWR	30	-	30	-	30	-	ns	

9.3.3 Timing Parameters for DDR5-5600 to DDR5-6400

The simulated timing parameters in this section are defined based on the nominal tCK(avg)min and in accordance with the rules in the Rounding Definitions and Algorithms section.

Table 9-5 DDR5-5600 to DDR5-6400

Speed		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock cycle									
Average Clock Period	tCK(avg)	0.357	-	0.333	-	0.312	-	ns	1
Command and Address Timing									
Read Command Delay within Same Bank Group	tCCD_L	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Write command delay (same bank group)	tCCD_L_WR	Max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	nCK,ns	

Write command delay (same bank group), second write without read/write operation	tCCD_L_WR2	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	nCK,ns	
Read-to-write command delay, same bank group Same bank group	tCCD_L_RTWW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,ns	3,5,6
Write-to-read command delay, same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read-to-read command delay, different bank group	tCCD_S	8	-	8	-	8	-	nCK	
Delay									
Write command delay (for different bank group)	tCCD_S_WR	8	-	8	-	8	-	nCK	
Read-to-Write command delay for different bank groups	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,ns	3,5,6
Write-to-Read command delay for different bank groups	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write-to-Read (auto mode) Precharge command delay for same bank	tCCD_WTRA	CWL+ WBL/2 + tWR - tRTP						nCK,ns	2,4,6
Activate-to-Activate command Activate-to-Activate command delay to same bank group, 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Activation to activation command delay to same bank group (2KB page size) (2KB page size)	tRRD_L(2K)	Max (8nCK, 5ns)	-	Max (8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,ns	
Activate-to-Activate command delay, different bank groups 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	
Activate-to-Activate command delay, different bank groups Activate-to-activate command delay to different bank groups, 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	
Four Bank Activation Window, 1KB page size	tFAW (1K)	Maximum (32nCK, 11.428ns)	-	Maximum(32nCK, 10.666ns)	-	Maximum(32nCK, 10.000ns)	-	nCK, ns	
Four-Activation Window for 2KB Page Size	tFAW (2K)	Maximum(40nCK, 14.285ns)	-	Maximum(40 nCK, 13.333 ns)	-	Maximum(40 nCK, 12.500 ns)	-	nCK, ns	
Read to Precharge Command Delay	tRTP	Max (12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to precharge command delay	tPPD	2	-	2	-	2	-	nCK	7
Write recovery time	tWR	30	-	30	-	30	-	ns	

Note 1: The listed tCK(avg)min values are for reference only. Please refer to the "Speed Bin and Operation" section for all valid tCK(avg) values.

Note 2: tCCD_WTRA(min) must always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithm, nCCD_WTRA(min) must always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

Note 3: RBL: Read burst length associated with read command. RBL = 32 (36 when RCRC enabled) applies to fixed BL32 and BL32 in BL32 OTF mode. RBL = 16 (18 when RCRC enabled) applies to fixed BL16 and BL16 in BL32 OTF mode. RBL = 16 (18 when RCRC enabled), applies to BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.

Note 4: WBL: Write burst length associated with a write command. WBL = 32 (36 with WCRC on) applies to fixed BL32 and BL32 in BL32 OTF mode.

WBL = 16 (18 with WCRC on) applies to fixed BL16 and BL16 reads in BL32 OTF mode. DQS offset timing may affect tRTW timing; when the suffix is 1.5tCK, an additional 1tCK must be added.

Note 5: CWL = CL - 2

Note 6: tPPD applies to any precharge command pair (PREab, PREsb, PREpb). tPPD also applies to any precharge command pair for different dies in 3DS DDR5 SDRAM.

9.3.4 Timing Parameters for DDR5-6800 through DDR5-7600

Table 9-6 applies to DDR5-6800 through DDR5-7600

Speed		DDR5-6800		DDR5-7200		DDR5-7600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Read-to-Read command delay (same bank group)									

Read-to-Read command delay (same bank group)	tCCD_L	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK	34
Write-to-Write Command Delay, Same Bank Group	tCCD_L_WR	max(32nCK, 20ns)		max(32nCK, 20ns)		Max(32nCK, 20ns)		ns	
Read-to-Read command delay (different bank groups)	tCCD_S	8	-	8	-	8	-	nCK	34
Activate-to-Activate command delay, different bank groups, 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	34
Activate-to-Activate command delay, different ACTIVATE-to-ACTIVATE command delay, different bank group, 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	34
ACTIVATE-to-ACTIVATE command delay, same bank group, 2KB page size bank group, 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK	34
ACTIVATE-to-ACTIVATE command delay, same bank group, 1KB page size same bank group (1KB page size)	tRRD_L(1K)	Max (8nCK, 5ns)	-	max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK	34
Four-Activation Window for 2KB Page Size	tFAW(2K)	max(40nCK, xxns)	-	Maximum (40nCK, xxns)	-	max(40nCK, xxns)	-	nCK,ns	34
Four Bank Activation Window, 1KB page size	tFAW(1K)	max(32nCK, xxns)	-	Maximum (32nCK, xxns)	-	max(32nCK, xxns)	-	nCK,ns	34
Delay from start of internal write transaction to internal read command	tWTR_S	2.5	-	2.5	-	2.5	-	ns	1,2,e, 34
Write to Read Command Delay, Same Bank Group	tWTR_L	10	-	10	-	10	-	ns	1,34
Read to Precharge Command Delay	tRTP	7.5	-	7.5	-	7.5	-	ns	
Precharge to precharge command delay	tPPD	2	-	2	-	2	-	nCK (average)	
Write recovery time	tWR	TBD	-	TBD	-	TBD	-	ns	1

9.3.5 Timing Parameters for DDR5-8000 to DDR5-8400

Table 9-7 DDR5-8000 to DDR5-8400

Speed		DDR5-8000		DDR5-8400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Command and Address Timing							
Read-to-Read Command Delay, Same Bank Group	tCCD_L	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK	34
Write-to-Write Command Delay, Same Bank Group	tCCD_L_WR	max(32nCK, 20ns)		max(32nCK, 20ns)		ns	
Read-to-Write Command Delay, Different Bank Groups	tCCD_S	8	-	8	-	nCK	34
Activate to activate command delay to different bank groups, 2KB page size Activate to activate command delay to different bank groups (2KB page size)	tRRD_S(2K)	8	-	8	-	nCK	34

Activate to activate command Activate to activate command delay to different bank groups (1KB page size)	tRRD_S(1K)	8	-	8	-	nCK	34
Activate to activate command delay to same bank group group, applicable to 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK	34
Activate to activate command delay (same bank group) 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK	34
Four-Activation Window for 2KB Page Size	tFAW(2K)	Maximum (40nCK, xxns)	-	Maximum (40nCK, xxns)	-	nCK,ns	34

Four-Activation Window for 1KB Page Size	tFAW(1K)	Maximum (32nCK, xxns)	-	Maximum (32nCK, xxns)	-	nCK,ns	34
Write-to-Read Command Delay for Same Bank Group	tWTR_S	2.5	-	2.5	-	ns	1,2,e,34
Delay from the Start of Internal Write Transaction to Internal Read Command (Same Bank Group)	tWTR_L	10	-	10	-	ns	1,34
Precharge command delay	tRTP	7.5	-	7.5	-	ns	
Precharge to precharge command delay	tPPD	2	-	2	-	nCK (average)	
Write recovery time	tWR	TBD	-	TBD	-	ns	1

9.3.6 Timing parameters for 3DS-DDR5-3200 to 3DS-DDR5-4000 x4 2H & 4H

Analog timing parameters defined in this section shall be accurate to 1 ps. The minimum values of parameters that vary with tCKmin shall refer to the corresponding data rate.

Table 9-8 Definition of tCKmin Values

Applicable for x4 2H & 4H 3DS-DDR5-3200 to 3DS-DDR5-4000

Speed		DDR5-3200		DDR5-3600		DDR5-4000		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock cycle									
Average Clock Period	tCK(avg)	0.625	-	0.555	-	0.500	-	ns	1
3DS Command and Address Timing									
Read-to-Read Command Delay within Same Bank Group in Same Logic Rank	tCCD_L_slr	Max (8nCK, 5ns)	-	Max (8nCK, 5ns)	-	Max (8nCK, 5ns)	-	nCK, ns	
Write-to-Write command delay within same bank group of same logical rank Write-to-Write command delay within same bank group of same logical rank	tCCD_L_WR_slr	Max (32nCK,20ns)	-	Max (32nCK,20ns)	-	Max (32nCK,20ns)	-	nCK, ns	
Second Write command delay for same bank group within same logic rank (non-RMW)	tCCD_L_WR2_slr	Max (16nCK,10ns)	-	Max (16nCK,10ns)	-	Max (16nCK,10ns)	-	nCK, ns	
Read-to-Write command delay for same bank group within same logic rank	tCCD_L_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK, ns	3,5,6
Write-to-Read command delay for same bank group within same logic rank	tCCD_L_WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK, ns	4,6
Read-to-read command delay for different bank groups in same logic subrank	tCCD_S_slr	8	-	8	-	8	-	nCK	
Write command delay for different bank groups within a same logic rank	tCCD_S_WR_slr	8	-	8	-	8	-	nCK	
Read-to-Write command delay for different bank groups within a same logic rank	tCCD_S_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK, ns	3,5,6

Write-to-Read command delay for different bank groups within the same logical rank	tCCD_S_WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
Write-to-Read command delay with auto precharge for a same bank within a same logic rank	tCCD_WTRA_slr	CWL+ WBL/2+ tWR_slr - tRTP_slr						nCK, ns	2,4,6
Activate to activate command delay to same Activate to activate command delay to same bank group in same logic rank	tRRD_L_slr(1K)	Max (8nCK, 5ns)	-	Max (8nCK, 5ns)	-	Max (8nCK, 5ns)	-	nCK, ns	
Activate to activate command delay to different bank group in same logic rank	tRRD_S_slr(1K)	8	-	8	-	8	-	nCK	
Four activate window in same logic rank	tFAW_slr(1K)	Max (32nCK ,20.000ns)	-	Max (32nCK ,17.777 ns)	-	max(32nCK ,16.000ns)	-	nCK, ns	9
Read to precharge command delay within same logic rank	tRTP_slr	Max (12nCK, 7.5ns)	-	Max (12nCK, 7.5ns)	-	Max (12nCK, 7.5ns)	-	nCK,	
Precharge to Precharge Delay within Same Logic Level	tPPD_slr	2	-	2	-	2	-	nCK	7
Write Recovery Time within Same Logic Level	tWR_slr	30	-	30	-	30	-	ns	
Read to Read Command Delay Between Different Logic Levels	tCCD_dlr	Max (8nCK, 3.636ns)	-	Max (8nCK, 3.333ns))	-	Max (8nCK, 3.333ns)	-	nCK, ns	
Write command delay between different logical ranks	tCCD_WR_dlr	Max (8nCK, 3.636ns)	-	Max (8nCK, 3.333ns)	-	Max (8nCK, 3.333ns)	-	nCK, ns	12
Read-to-write command delay between different logical ranks	tCCD_RTW_dlr	CL - CWL + BL/2 + 2tCK - Read DQS offset +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6
Write-to-read command delay between different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
Activate-to-activate command delay between different logical ranks	tRRD_dlr	Max (4nCK, 1.818ns)	-	Max (4nCK, 1.666ns)	-	Max (4nCK, 1.666ns)	-	nCK, ns	
Four Activate Window across logical ranks	tFAW_dlr	Max (16nCK, 7.272ns)	-	Max (16nCK, 6.666ns)	-	Max (16nCK, 6.666ns)	-	nCK, ns	
Precharge to precharge delay for different logical ranks	tPPD_dlr	2	-	2	-	2	-	nCK	7
WRITE-to-WRITE command delay across different physical channels	tCCD_WR_dpr	8	-	8	-	8	-	nCK	12,13
DIMM Channel Active Window	tDCAW	128	-	128	-	128	-	nCK	10,11, 13,14
DIMM Channel Activation Command Counter tDCAW	nDCAC	-	32	-	32	-	32	ACT	10,11,

9.3.7 Timing Parameters for 3DS-DDR5-4400 to 3DS-DDR5-5200 x4 2H & 4H

Analog timing parameters defined in this section require 1 ps accuracy. The minimum values for parameters that vary with tCKmin shall be defined based on the tCKmin of the corresponding data rate.

Table 9-9 applies to x4 2H and 4H 3DS-DDR5-4400 to 3DS-DDR5-5200

Speed		DDR5-4400		DDR5-4800		DDR5-5200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock cycle									
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384	-	ns	1
3DS Command and Address Timing									
Read-to-Read command delay for same bank group within same logic rank	tCCD_L_slr	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, TBD) 5ns)	-	nCK, ns	
Write-to-Write command delay for same bank group within same logic rank logical rank	tCCD_L_WR_slr	max(32nCK,20ns) ,20ns)	-	Max(32nCK ,20ns)	-	max(32nCK, 20ns) ,20ns)	-	nCK, ns	
Write command delay for same bank group in same logic die, second write (no read-modify-write) RMW	tCCD_L_WR2_slr	max(16nCK,10ns) ,10ns)	-	Max (16nCK ,10ns)	-	Max (16nCK ,10ns)	-	nCK, ns	
read-write command delay for same bank group within same logical rank logical rank	tCCD_L_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6
write-to-read command delay same bank group within same logical rank	tCCD_L_WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK, ns	4,6
read-to-read command delay for different bank groups within same logical rank	tCCD_S_slr	8	-	8	-	8	-	nCK	
write command delay for different bank groups within same logical rank logical rank write latency	tCCD_S_WR_slr	8	-	8	-	8	-	nCK	
Read-to-Write command delay for same bank group, same logical rank	tCCD_S_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6
Write-to-Read command delay Write-to-Read command delay for same bank group, same logical rank	tCCD_S_WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
Write-to-Read with Auto Precharge command Write-to-Read with Auto Precharge command delay for same logical rank	tCCD_WTRA_slr	CWL+ WBL/2+ tWR_slr - tRTP_slr						nCK,n s	2,4,6
Activate-to-Activate command delay for same bank group, same logical rank	tRRD_L_slr(1K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK, ns	
Activate to activate command delay for same bank group within the same logic rank	tRRD_S_slr(1K)	8	-	8	-	8	-	nCK	
Four activate windows (same logic level)	tFAW_slr(1K)	Max(32nCK ,14.545ns)	-	Max(32nCK max(32nCK, 13.333ns)	-	Max (32nCK Max(32nCK,12.307ns)	-	nCK, ns	9
Read command to precharge Command delay within the same logical rank	tRTP_slr	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max Max(12nCK, 7.5ns)	-	nCK, ns	

Precharge interval delay within the same logical rank	tPPD_slr	2	-	2	-	2	-	nCK	7
Write recovery time (same logical rank)	tWR_slr	30	-	30	-	30	-	ns	
Read-to-read command delay across different logic ranks	tCCD_dlr	MAX(8nCK, 3.636ns)	-	MAX(8nCK, 3.333ns)	-	MAX(8nCK, 3.333ns)	-	nCK	
Write-to-write command delay across different logic ranks	tCCD_WR_dlr	MAX(8nCK, 3.636ns)	-	Max(8nCK, 3.333ns)	-	Max(8nCK, 3.333ns)	-	nCK, ns	12
tCCD_RTW_dlr	tCCD_RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6
tCCD_WTR_dlr	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
tRRD_S_ slr(1K)	tRRD_dlr	Max(4nCK, 1.818ns)	-	Max (4nCK, 1.666ns)	-	Max (4nCK, 1.666ns)	-	nCK, ns	
Four-activation window for different logical ranks	tFAW_dlr	Max(16nCK, 7.272ns)	-	Max(16nCK, 6.666ns) (Correct if this column is DDR5-4800, otherwise adjust)	-	Max(16nCK, 6.666ns)	-	nCK, ns	

Precharge interval delay (between different logical ranks) for different logical ranks	tPPD_dlr	2	-	2	-	2	-	nCK	7
Minimum write command Write to different physical ranks	tCCD_ WR_dpr	8	-	8		8		nCK	12,13
DIMM channel activation window	tDCAW	128	-	128	-	128	-	nCK	10,11, 13,14
DIMM Channel Activation Command Counter tDCAW	nDCAC	-	32	-	32	-	32	ACT	10,11, 13,14

9.3.8 Timing parameters for 3DS-DDR5-4400 to 3DS-DDR5-5200 x4 2H & 4H

The analog timing parameters defined in this section shall be accurate to 1 ps. The minimum values of parameters that vary with tCKmin shall be defined using tCKmin at the relevant data rates for x4 2H and 4H.

Table 9-10 3DS-DDR5-5600 to 3DS-DDR5-6400

Speed		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.357	-	0.333	-	0.312	-	ns	1
3DS Command and Address Timing									
Read to Read Command Delay for Same Bank Group within Same Logical Rank	tCCD_L_slr	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK, ns	
Write Command Delay for Same Bank Group within Same Logical Rank	tCCD_L _ WR_slr	Max(32nCK ,20ns)	-	Max(32nCK ,20ns)	-	Max(32nCK ,20ns)	-	nCK, ns	
Write command delay for same bank group within a logic rank Write command delay for same bank group within a logic rank, second write non-RMW	tCCD_L_ WR2_slr	Max (16nCK ,10ns)	-	Max (16nCK ,10ns)	-	Max (16nCK ,10ns)	-	nCK, ns	
Read-to-write command delay for same bank group in same logic subrank	tCCD_L _ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6
Write-to-read command delay for same bank group in same logic subrank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK, ns	4,6
Read-to-read command delay for different bank groups in same logic subrank Read-to-read command delay for different bank groups in same logic subrank	tCCD_S_slr	8	-	8	-	8	-	nCK	
Write command delay Same logic subrank, different bank group	tCCD_S _ WR_slr	8	-	8	-	8	-	nCK	
Read-to-write command delay Read-to-Write command delay for different bank groups within the same logical rank	tCCD_S _ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6

Write-to-Read command delay for different bank groups within the same logical rank	tCCD_S _ WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,n s	4,6
Write-to-Read command delay (with auto precharge) The same bank within the same logical rank	tCCD_ WTRA_slr	CWL+ WBL/2+ tWR_slr - tRTP_slr						nCK,n s	2,4,6
Activate-to-Activate command delay for the same bank group within the same logical rank same logical rank	tRRD_L _ slr(1K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK,n s	
Command delay for different bank groups within the same logic level Logical rank	tRRD_S _ slr(1K)	8	-	8	-	8	-	nCK	
Four activate windows (same logic level)	tFAW _ slr(1K)	Max(32nCK ,11.428 ns)	-	Max(32nCK Max(32nCK ,10.666ns)	-	Max (32nCK Max(32nCK, 10.000ns)	-	nCK, ns	9
Read command to precharge command delay (within same logical rank)	tRTP_slr	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,n s	
Precharge command to precharge command delay (within same logical rank) same logical rank	tPPD_slr	2	-	2	-	2	-	nCK	7
Write recovery time (same logical rank)	tWR_slr	30	-	30	-	30	-	ns	
Read command delay (different logical ranks)	tCCD_dlr	Max(8nCK, 3.214ns)	-	Max(8nCK, 3.214ns)	-	max(8nCK, 3.125ns)	-	nCK	
Write command delay (different logical ranks)	tCCD_ WR_dlr	max(8nCK, 3.214 ns)	-	Max(8nCK, 3.214ns)	-	Max(8nCK, 3.125 ns)	-	nCK, ns	12
tCCD_RTW_dlr	tCCD_ RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) +(tRPST - 0.5tCK)+ tWPRE						nCK,n s	3,5,6
tCCD_WTR_dlr	tCCD_ WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK, ns	4,6
tRRD_S_ slr(1K)	tRRD_dlr	Max (4nCK, 1.666ns)	-	Max (4nCK, 1.666ns)	-	Max (4nCK, 1.666ns)	-	nCK, ns	
Four activate windows for different logical ranks Logical rank	tFAW_dlr	Max (16nCK Max (16nCK,6.666ns)	-	Max (16nCK ,6.666ns)	-	Max (16nCK ,6.666ns)	-	nCK, ns	
Precharge to precharge delay for different logical ranks	tPPD_dlr	2	-	2	-	2	-	nCK	7
Write-to-Write Command Delay across Different Physical Ranks	tCCD_ WR_dpr	8	-	8	-	8	-	nCK	12,13
DIMM Channel Activation Window	tDCAW	128	-	128	-	128	-	nCK	10,11, 13,14

DIMM Channel Activation Command Counter tDCAW	nDCAC	-	32	-	32	-	32	ACT	10,11, 13,1

Note 1: The listed minimum average clock period (tCK(avg)) values are for reference only. Refer to the "Speed Bins and Operation" section for all valid average clock period (tCK(avg)) values.
Note 2: tCCD_WTRA_slr(min) must always be greater than or equal to CWL + WBL/2 + tWR_slr(min) - tRTP_slr(min), and when using the appropriate rounding algorithm,
tCCD_WTRA_slr(min) must always be greater than or equal to CWL + WBL/2 + tWR_slr(min) - tRTP_slr(min).
Note 3: RBL: Read Burst Length associated with read commands. RBL = 32 (fixed BL32 and BL32 in BL32 OTF mode) RBL = 16 (fixed BL16 and BL16 in
BL32 OTF mode) RBL = 16 (BL16 in BC8 OTF mode, and BC8 in BC8 OTF mode)
Note 4: WBL: Write burst length associated with write commands. WBL = 32 (when BL32 is fixed and BL32 is in BL32 OTF mode); WBL = 16 (when BL16 is fixed and BL16 is in BL16 OTF mode); WBL = 16 applies to BL16 in BC8 OTF mode and BC8 in BC8 mode.
Note 5: The following factors must be considered in the tRTW equation: because tDQS2CK requires adding 1 tCK for read DQS offset timing, it may affect the tRTW timing. When the suffix is 1.5 tCK, the timing must be increased.
1tCK
Note 6: CWL = CL - 2
Note 7: tPPD applies to any precharge command combination (PREab, PREsb, PREpb). tPPD also applies to precharge command combinations targeting different dies in 3DS DDR5 SDRAM.
Note 8: The timings listed in this table apply to x4
2H and 4H 3D devices. Note 9: Applies only to x4
devices. Timings for x8 devices are TBD.
Note 10: Activate commands to different logical ranks within the same package may be issued simultaneously in the same cycle.
Note 11: Activate commands to the same subchannel on the same logical rank are limited by tDCAW. Within the tDCAW period, a maximum of nDCAC activate commands can be received on the same subchannel of the same logical rank.